Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2023/24)
Machine Structures 2 course
Kara Abdelaziz professor

Machine Structures 2 catch up exam solution

Exercise 1 : (4 points)

1. Digital electronics are electronics where logical values 0 and 1 are the main circuit signals. **(1 point)**

2. The truth table and the logical expression of a tristate buffer : **(1 point)**

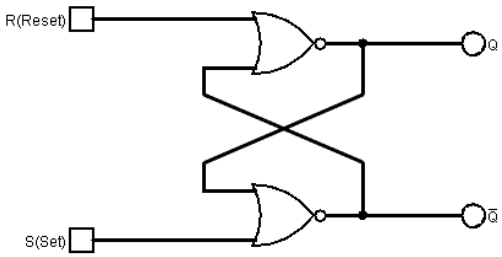
A	C	S
0	0	Z
1	0	Z
0	1	0
1	1	1

logical expression :

$$\begin{cases} if\,(C=0) \Rightarrow S=Z \\ if\,(C=1) \Rightarrow S=A \end{cases}$$

3. The difference between synchronous and asynchronous sequential circuits, is that the synchronous keep track of the clock while executing. Whereas, the asynchronous don't. **(1 point)**

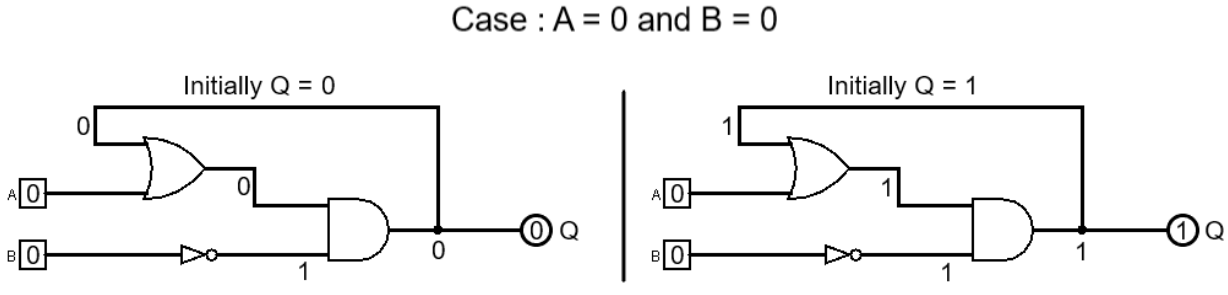
4. The schematics of RS-Latch and its truth table : **(1 point)**



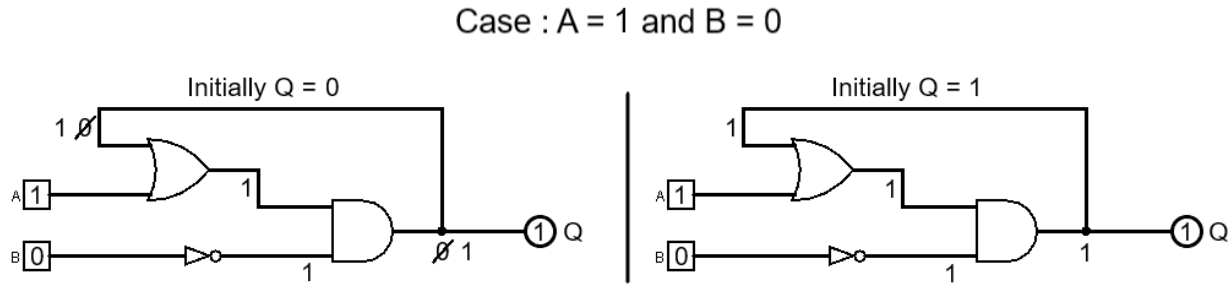
R	S	Q	$\overline{Q}$
1	0	0	1
0	1	1	0
0	0	Q`	$\overline{Q}$`
1	1	0	0

Exercise 2 : (5 points)

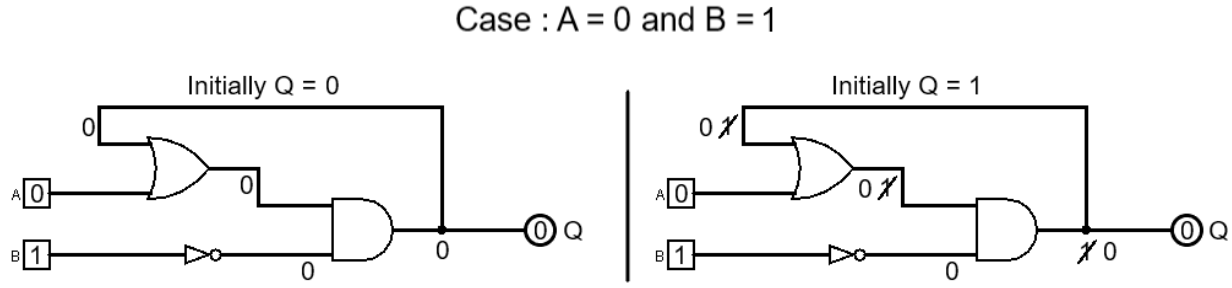
Case A = 0 and B = 0 : (1 point)



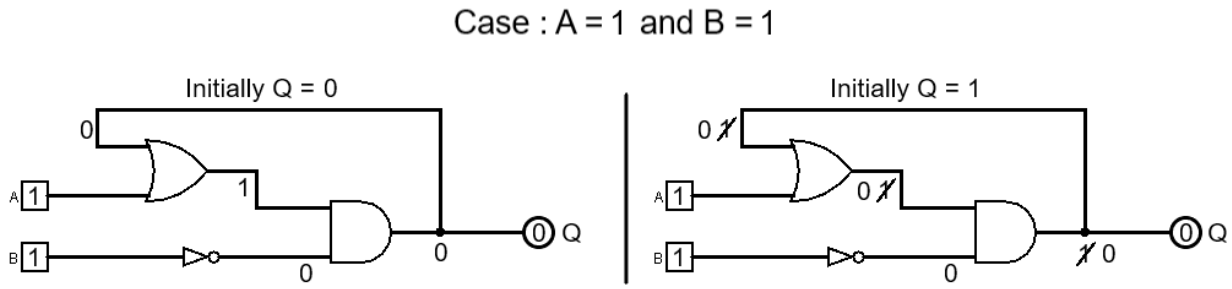
Case A = 1 and B = 0 : (1 point)



Case A = 0 and B = 1 : (1 point)



Case A = 1 and B = 1 : (1 point)



The circuit truth table : **(0,5 point)**

A	B	Q	
0	0	Q'	Memorize
0	1	0	Reset to 0
1	0	1	Set to 1
1	1	0	Reset to 0

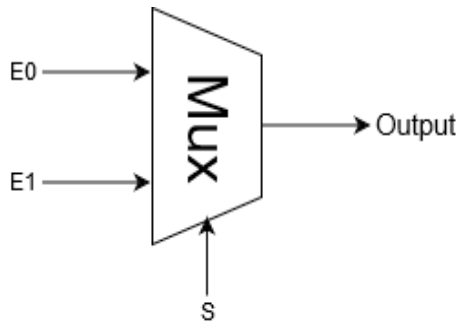
This asynchronous sequential circuit could be used as RS-Latch (A as Set and B as Reset) **(0,5 point)**

Note : Despite the case A=1, B=1 is a reset, the circuit is still an RS-Latch. Because the case (1,1) is not supposed to be used in an RS-Latch.

Exercise 3 : (5 points)

1. Mux 2-1 Multiplexer :

Step 1 : Global Scheme **(0,5 point)**



Step 2 : Truth Table **(0,5 point)**

E0	E1	S	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Step 3 : Canonical Disjunctive Functions **(0,5 point)**

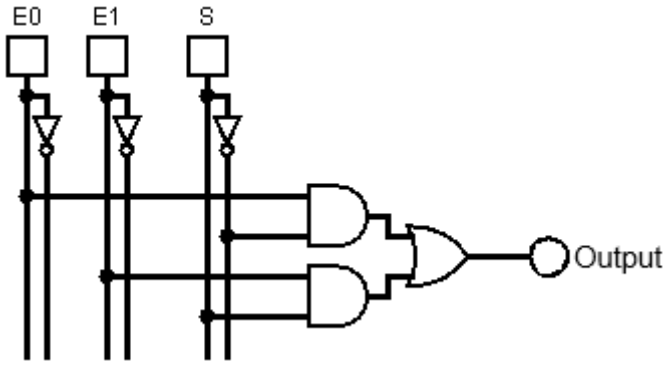
Output(E0,E1,S) = $\overline{E0}\cdot E1\cdot S + E0\cdot\overline{E1}\cdot\overline{S} + E0\cdot E1\cdot\overline{S} + E0\cdot E1\cdot S$

Step 4 : Karnaugh Map **(0,5 point)**

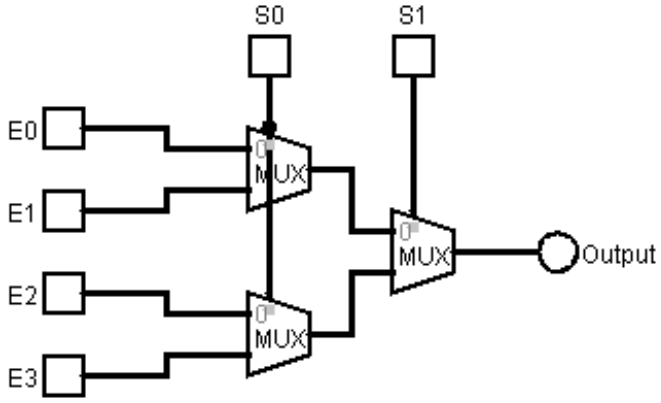
S \ E0E1	00	01	11	10
0	0	0	1	1
1	0	1	1	0

Output(E0,E1,S) = $E0\cdot\overline{S} + E1\cdot S$

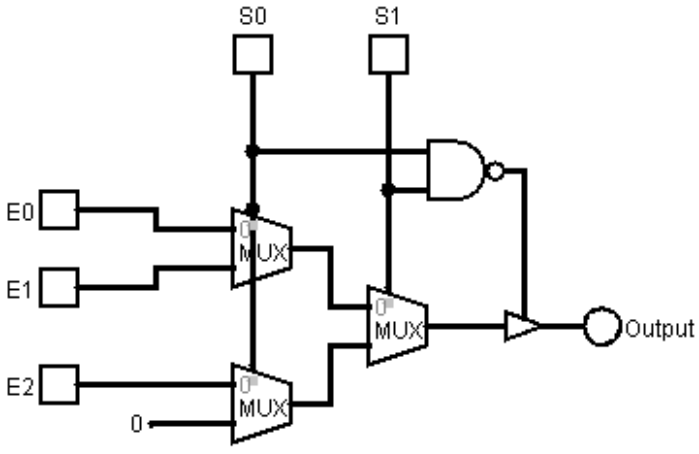
Step 5 : Schematics **(1 point)**



2. Mux 4-1 Multiplexer : **(1 point)**



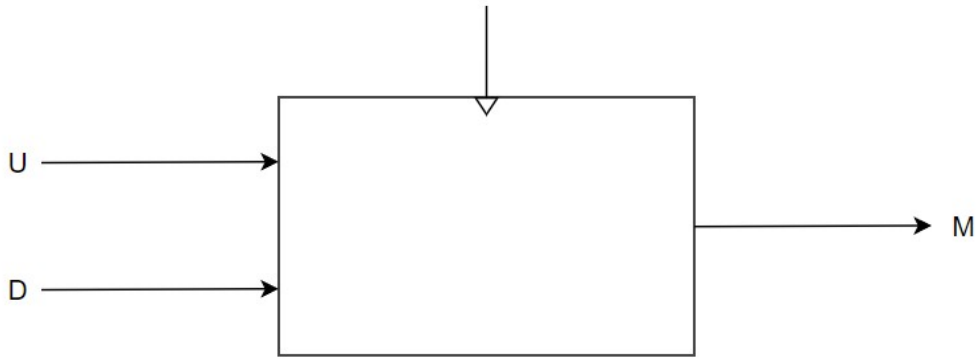
3. Mux 3-1 Multiplexer : **(1 point)**



Note : Putting only E3 to Z is not a valid solution. Because circuits don't behave normally with a Z value in their entries.

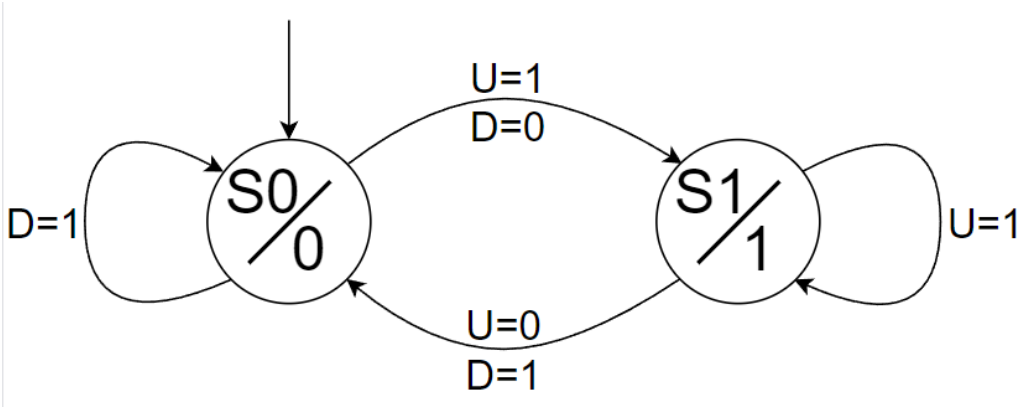
Exercise 4 : (6 + 1 bonus point)

Step 1 : Global Scheme **(1 point)**



U : for UP
D : for DOWN
M : for Motor

Step 2 : F.S.M. **(1 point)**



Step 3 : Transition Table **(1 point)**

Current State	U	D	Next State
S0	0	0	S0
S0	0	1	S0
S0	1	0	S1
S0	1	1	S0
S1	0	0	S1
S1	0	1	S0
S1	1	0	S1
S1	1	1	S1

Step 4 : Encoded States Table and Outputs Table **(1 point)**

State	S	M
S0	0	0
S1	1	1

Step 5 : Table de Transition Encodée **(1 point)**

S	U	D	S'
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Step 6 : Logical Functions **(1 point)**

M(S) = S (directly deducted)

D \ SU	00	01	11	10
00	0	1	1	1
01	0	0	1	0

$$S'(S,U,D) = U\cdot\overline{D} + S\cdot\overline{D} + S\cdot U$$

Step 7 : Schematics **(1 point)**