Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2023/24)
Machine Structures 2 course
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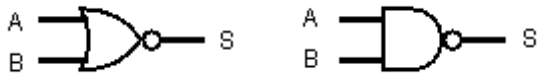
Machine Structures 2 exam solution

Exercise 1 : (4 points)

1. The main 2 values to represent information in digital systems are logic values 0 and 1. **(1 point)**

2. We have 2 universal gates : NAND and NOR symbolized as follow : **(0,5 point)**



They are called universal because using one of them, it is possible to reconstruct any possible digital circuit.**(0,5 point)**

3. The difference between Moore and Mealy machine regarding their output is that, Mealy machine outputs on State, and Mealy machine outputs on Transition. **(1 point)**

4. Truth Table of the circuit is as follow : **(1 point)**

A	B	S
0	0	1
0	1	0
1	0	0
1	1	1

Exercise 2 : (10 points)

1.

Step 1 : Global Scheme **(1 point)**

Step 2 : Truth Table **(1 point)**

E2	E1	E0	S3	S2	S1	S0
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	0	1	1	0
1	0	0	1	0	0	0
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	1	1	1	0

Step 3 : Disjunctive Canonical Functions **(1 point)**

$S3(E2,E1,E0) = E2\cdot\overline{E1}\cdot\overline{E0} + E2\cdot\overline{E1}\cdot E0 + E2\cdot E1\cdot\overline{E0} + E2\cdot E1\cdot E0$
$S2(E2,E1,E0) = \overline{E2}\cdot E1\cdot\overline{E0} + \overline{E2}\cdot E1\cdot E0 + E2\cdot E1\cdot\overline{E0} + E2\cdot E1\cdot E0$
$S1(E2,E1,E0) = \overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E2}\cdot E1\cdot E0 + E2\cdot\overline{E1}\cdot E0 + E2\cdot E1\cdot E0$
$S0(E2,E1,E0) = 0$ (don't require more reduction)

Step 4 : Karnaugh Map **(1 point)**

E0 \ E2E1	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$S3(E2,E1,E0) = E2$

E0 \ E2E1	00	01	11	10
0	1	1	1	1
1	1	1	1	1

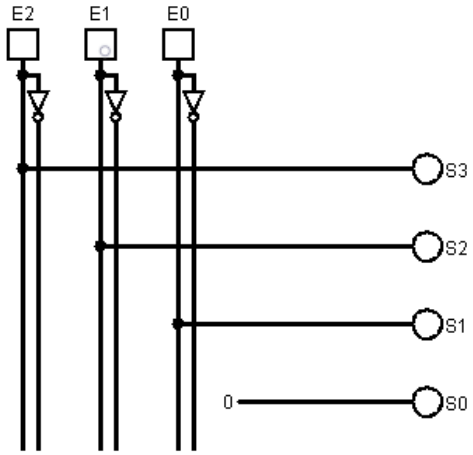
$S2(E2,E1,E0) = E1$

E0 \ E2E1	00	01	11	10
0	0	0	0	0
1	1	1	1	1

$S1(E2,E1,E0) = E0$

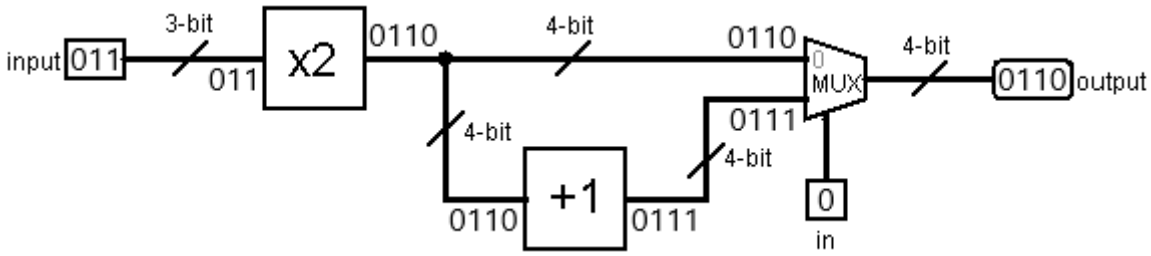
Note : This circuit is actually a left shifter of 1 bit.

Step 5 : Schematics **(1 point)**

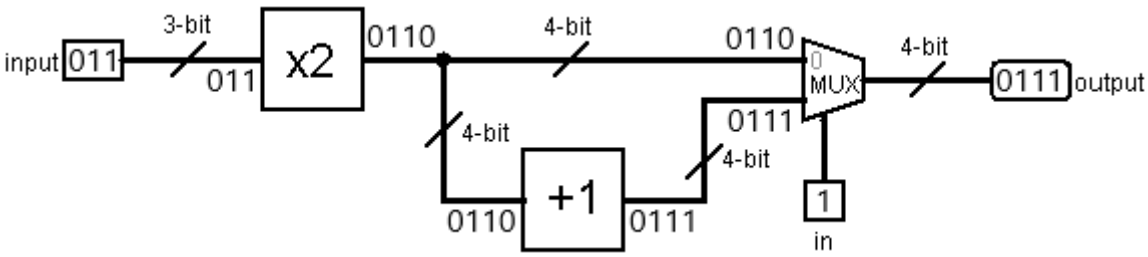


2. This circuit has no gates, then there is no universal transformation to do on it. **(2 point)**

3. The execution in the case of *n* = 0 : **(1 point)**



The execution in the case of *n* = 1 : **(1 point)**

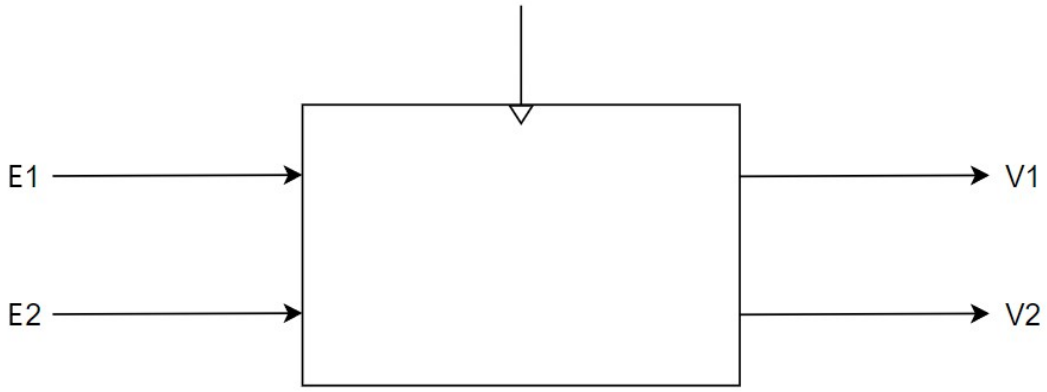


4. The mathematical formula for *n* = 0 is $y=2x$ and for *n* = 1 is $y=2x+1$ **(0,5 point)**

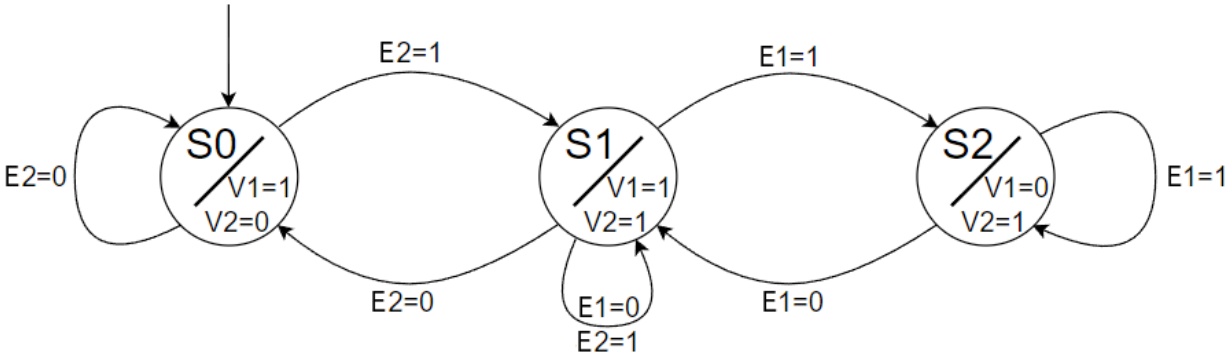
The purpose of the circuit is to generate *even* and *odd* numbers following the previous formulas. **(0,5 point)**

Exercise 3 : (6 + 1 points)

Step 1 : Global Scheme **(1 point)**



Step 2 : F.S.M. **(1 point)**



Step 3 : Transition Table (1 point)

Current State	E1	E2	Next State
S0	0	0	S0
S0	0	1	S1
S0	1	0	-
S0	1	1	-
S1	0	0	S0
S1	0	1	S1
S1	1	0	-
S1	1	1	S2
S2	0	0	-
S2	0	1	S1
S2	1	0	-
S2	1	1	S2

Step 4 : Encoded States Table and Outputs Table **(1 point)**

State	S_1	S_0	V1	V2
S0	0	0	1	0
S1	0	1	1	1
S2	1	0	0	1

Step 5 : Table de Transition Encodée **(1 point)**

S_1	S_0	E1	E2	S'_1	S'_0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	-	-
0	0	1	1	-	-
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	-	-
0	1	1	1	1	0
1	0	0	0	-	-
1	0	0	1	0	1
1	0	1	0	-	-
1	0	1	1	1	0

Note : The State S3 is an impossible state in the table, then it becomes *don't care*.

Step 6 : Logical Functions **(1 point)**

$V1(S_1,S_0) = \overline{S}_1$ (directly deducted)
$V2(S_1,S_0) = S_1+S_0$ (S3 is supposed *don't care.* Then, a xor $\oplus$ is also a correct answer)

S_1S_0 / E1E2	00	01	11	10
00	0	0	-	-
01	0	0	-	0
11	-	1	-	1
10	-	-	-	-

$S'_1(S_1,S_0,E1,E2) = E1 \cdot E2$

S_1S_0 / E1E2	00	01	11	10
00	0	0	-	-
01	1	1	-	1
11	-	0	-	0
10	-	-	-	-

$S'_0(S_1,S_0,E1,E2) = \overline{E1} \cdot E2$

Step 7 : Schematics **(1 point)**