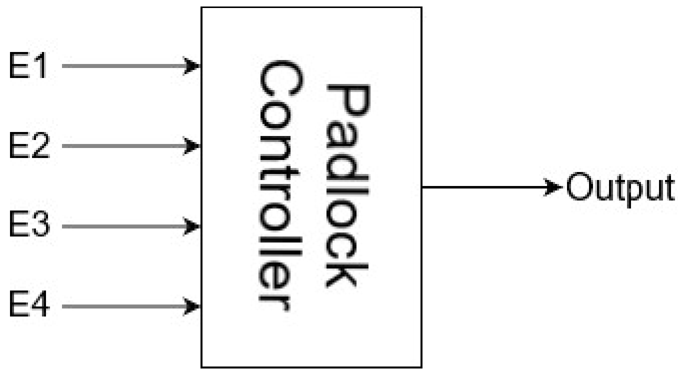
Sétif 1 University
Faculty of Sciences
Common Core Mathematics and Computer Science

2nd semester (year 2023/24)
Machine Structures 2 course
Kara Abdelaziz professor

Problem set 1 solution
(Combinational Circuits)

Exercise 01 :

Step 1 : Global Scheme



Step 2 : Truth Table

E1	E2	E3	E4	Output
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

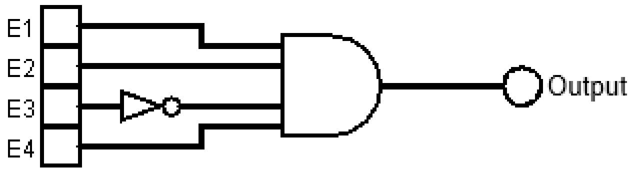
Step 3 : Disjunctive Canonical Functions

Output(E1,E2,E3,E4) = $E1 \cdot E2 \cdot \overline{E3} \cdot E4$

Étape 4 : Karnaugh Map

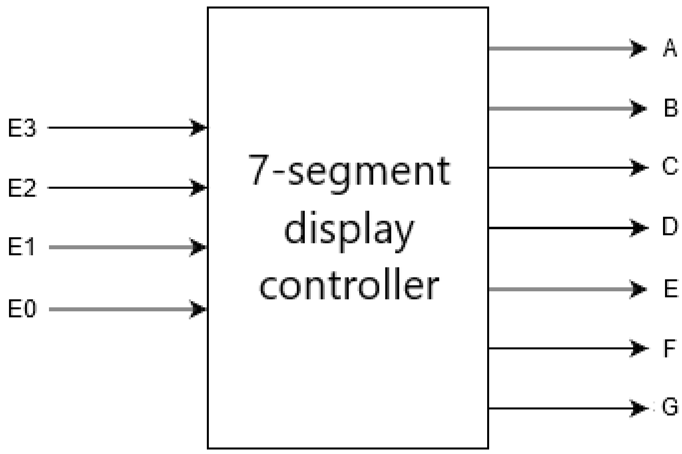
Not more simplification possible.

Step 5 : Schematics



Exercise 02 :

Step 1 : Global Scheme



Step 2 : Truth Table

E3	E2	E1	E0	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	-	-	-	-	-	-	-
1	0	1	1	-	-	-	-	-	-	-
1	1	0	0	-	-	-	-	-	-	-
1	1	0	1	-	-	-	-	-	-	-
1	1	1	0	-	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-	-

Step 3 : Disjunctive/Conjonctives Canonical Functions

$A(E3,E2,E1,E0) = (E3+E2+E1+\overline{E0})\cdot(E3+\overline{E2}+E1+E0)$
$B(E3,E2,E1,E0) = (E3+\overline{E2}+E1+\overline{E0})\cdot(E3+\overline{E2}+\overline{E1}+E0)$
$C(E3,E2,E1,E0) = (E3+E2+\overline{E1}+E0)$
$D(E3,E2,E1,E0) = (E3+E2+E1+\overline{E0})\cdot(E3+\overline{E2}+E1+E0)\cdot(E3+\overline{E2}+\overline{E1}+\overline{E0})$
$E(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0}$
$F(E3,E2,E1,E0) = (E3+E2+E1+\overline{E0})\cdot(E3+E2+\overline{E1}+E0)\cdot(E3+E2+\overline{E1}+\overline{E0})\cdot(E3+\overline{E2}+\overline{E1}+\overline{E0})$
$G(E3,E2,E1,E0) = (E3+E2+E1+E0)\cdot(E3+E2+E1+\overline{E0})\cdot(E3+\overline{E2}+\overline{E1}+\overline{E0})$

Step 4 : Karnaugh Map

E1E0 \ E3E2	00	01	11	10
00	1	0	-	1
01	0	1	-	1
11	1	1	-	-
10	1	1	-	-

$A(E3,E2,E1,E0) = (E3+E2+E1+\overline{E0})\cdot(\overline{E2}+E1+E0)$

E1E0 \ E3E2	00	01	11	10
00	1	1	-	1
01	1	0	-	1
11	1	1	-	-
10	1	0	-	-

$B(E3,E2,E1,E0) = (\overline{E2}+E1+\overline{E0})\cdot(\overline{E2}+\overline{E1}+E0)$

E1E0 \ E3E2	00	01	11	10
00	1	1	-	1
01	1	1	-	1
11	1	1	-	-
10	0	1	-	-

$C(E3,E2,E1,E0) = (E2+\overline{E1}+E0)$

E1E0 \ E3E2	00	01	11	10
00	1	0	-	1
01	0	1	-	1
11	1	0	-	-
10	1	1	-	-

$D(E3,E2,E1,E0) = (E3+E2+E1+\overline{E0})\cdot(\overline{E2}+E1+E0)\cdot(\overline{E2}+\overline{E1}+\overline{E0})$

E1E0 \ E3E2	00	01	11	10
00	1	0	-	1
01	0	0	-	0
11	0	0	-	-
10	1	1	-	-

$E(E3,E2,E1,E0) = E1\cdot\overline{E0} + \overline{E2}\cdot\overline{E0}$

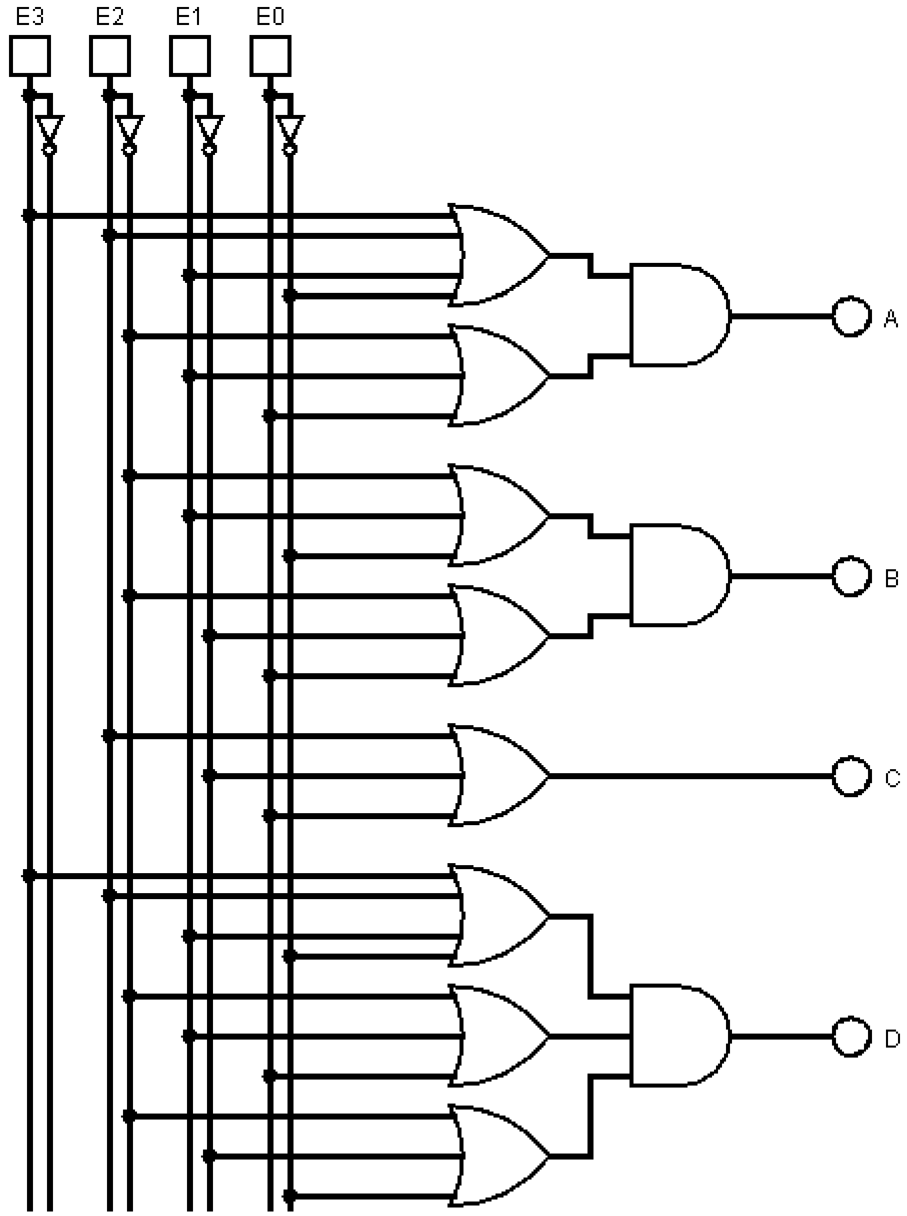
E1E0 \ E3E2	00	01	11	10
00	1	1	-	1
01	0	1	-	1
11	0	0	-	-
10	0	1	-	-

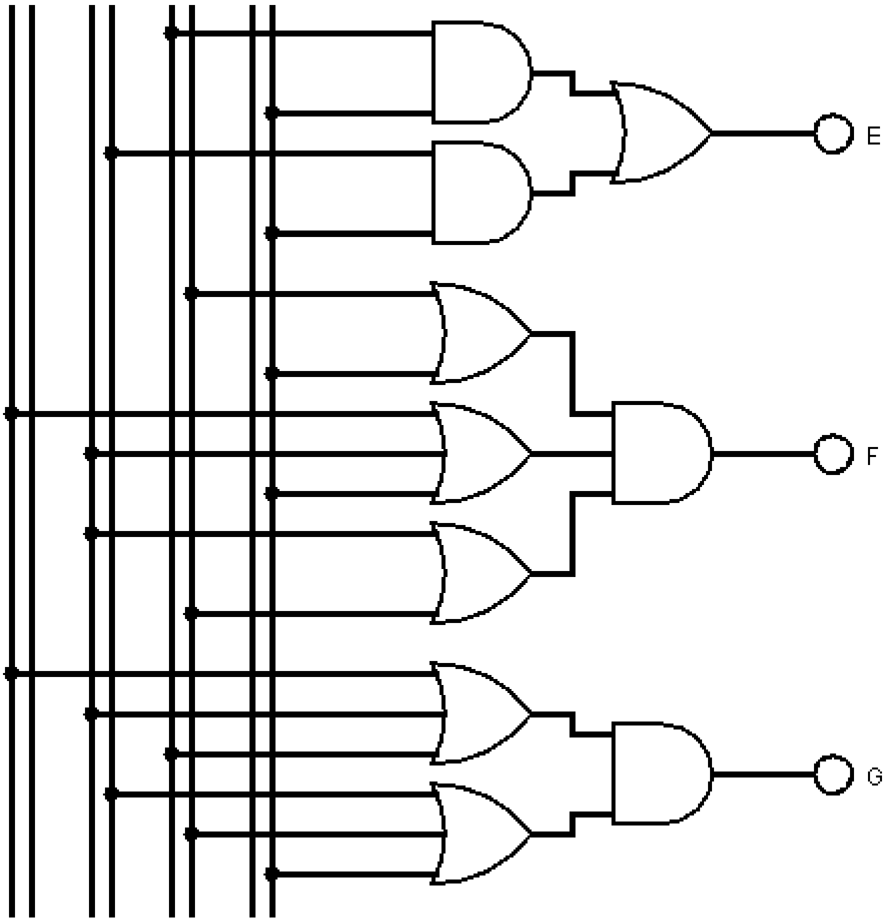
$F(E3,E2,E1,E0) =(\overline{E1}+\overline{E0})\cdot(E3+E2+\overline{E0})\cdot(E2+\overline{E1})$

E1E0 \ E3E2	00	01	11	10
00	0	1	-	1
01	0	1	-	1
11	1	0	-	-
10	1	1	-	-

$$G(E3,E2,E1,E0) = (E3+E2+E1)\cdot(\overline{E2}+\overline{E1}+\overline{E0})$$

Step 5 : Schematics



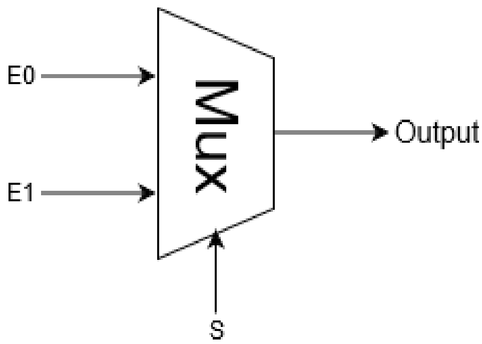


Exercise 03 :

1)

Multiplexer :

Step 1 : Global Scheme



Step 2 : Truth Table

E0	E1	S	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Step 3 : Canonical Disjunctive Functions

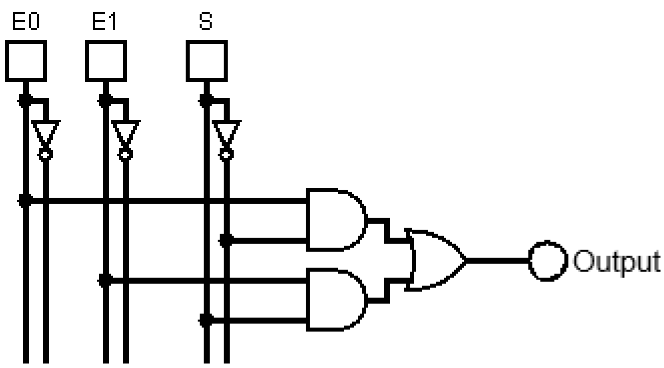
Output(E0,E1,S) = $\overline{E0}\cdot E1\cdot S + E0\cdot\overline{E1}\cdot\overline{S} + E0\cdot E1\cdot\overline{S} + E0\cdot E1\cdot S$

Step 4 : Karnaugh Map

S \ E0E1	00	01	11	10
0	0	0	1	1
1	0	1	1	0

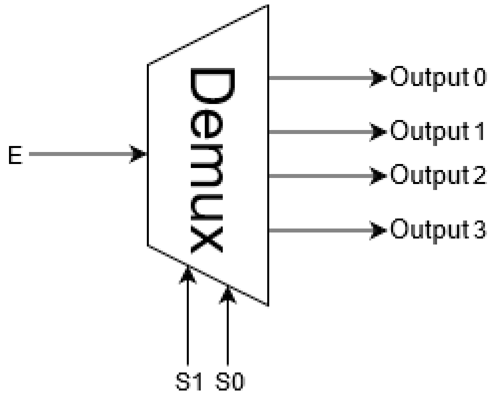
Output(E0,E1,S) = $E0\cdot\overline{S} + E1\cdot S$

Step 5 : Schematics



Demultiplexer :

Step 1 : Global Scheme



Step 2 : Truth Table

E	S1	S0	Output0	Output1	Output2	Output3
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

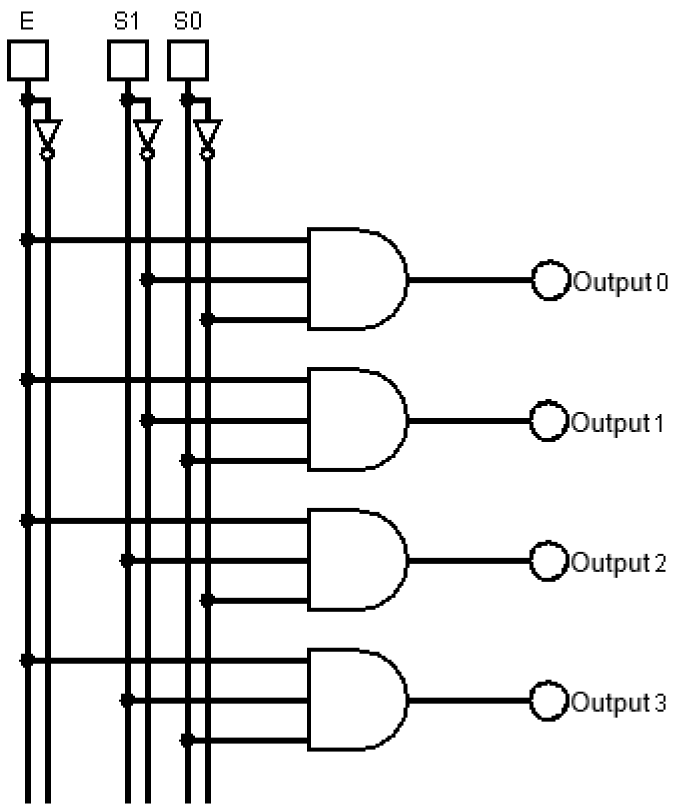
Step 3 : Canonical Disjunctive Functions

Output0(E,S1,S0) = $E \cdot \overline{S1} \cdot \overline{S0}$
Output1(E,S1,S0) = $E \cdot \overline{S1} \cdot S0$
Output2(E,S1,S0) = $E \cdot S1 \cdot \overline{S0}$
Output3(E,S1,S0) = $E \cdot S1 \cdot S0$

Step 4 : Karnaugh Map

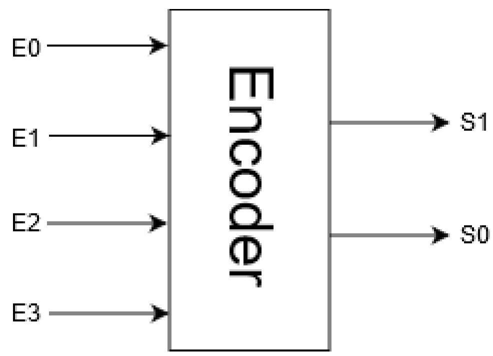
No more possible simplification.

Step 5 : Schematics



Encoder :

Step 1 : Global Scheme



Step 2 : Truth Table

E3	E2	E1	E0	S1	S0
0	0	0	0	-	-
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	-	-
0	1	0	0	1	0
0	1	0	1	-	-
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	1	1
1	0	0	1	-	-
1	0	1	0	-	-
1	0	1	1	-	-
1	1	0	0	-	-
1	1	0	1	-	-
1	1	1	0	-	-
1	1	1	1	-	-

Step 3 : Canonical Disjunctive Functions

S0(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0}$
S1(E3,E2,E1,E0) = $\overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0}$

Step 4 : Karnaugh Map

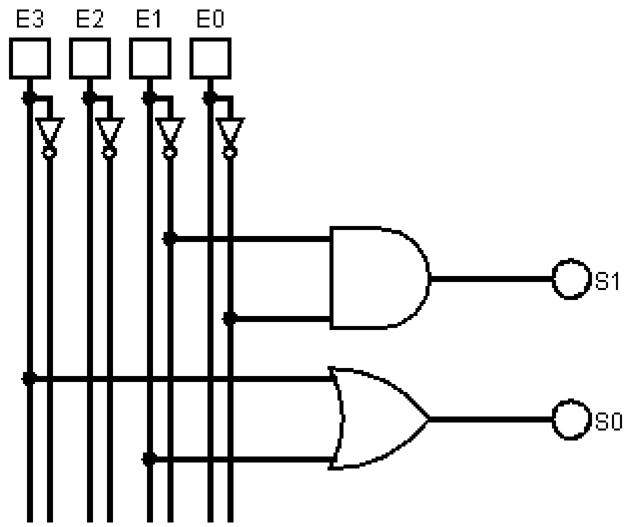
E1E0 \ E3E2	00	01	11	10
00	-	0	-	1
01	0	-	-	-
11	-	-	-	-
10	1	-	-	-

S0(E3,E2,E1,E0) = E3 + E1

E1E0 \ E3E2	00	01	11	10
00	-	1	-	1
01	0	-	-	-
11	-	-	-	-
10	0	-	-	-

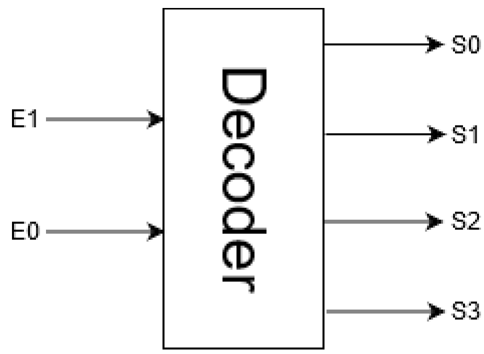
S1(E3,E2,E1,E0) = $\overline{E1}\cdot\overline{E0}$

Step 5 : Schematics



Decoder :

Step 1 : Global Scheme



Step 2 : Truth Table

E1	E0	S0	S1	S2	S3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

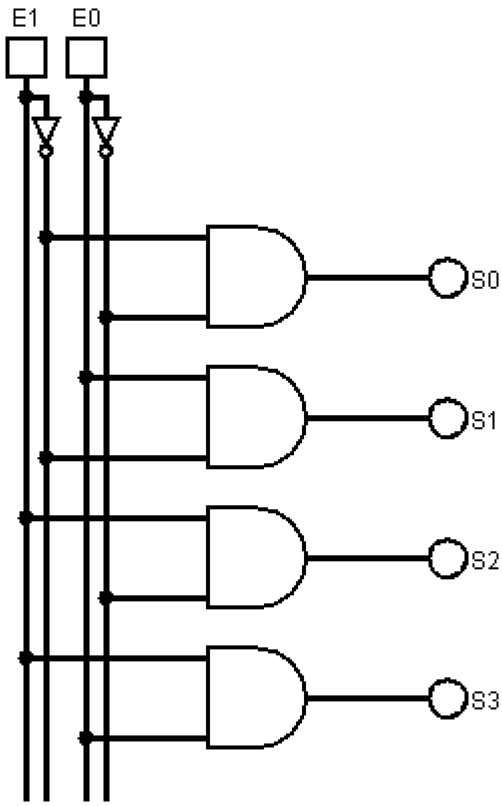
Step 3 : Canonical Disjunctive Functions

$S0(E1,E0) = \overline{E1}\cdot\overline{E0}$
$S1(E1,E0) = \overline{E1}\cdot E0$
$S2(E1,E0) = E1\cdot\overline{E0}$
$S3(E1,E0) = E1\cdot E0$

Step 4 : Karnaugh Map

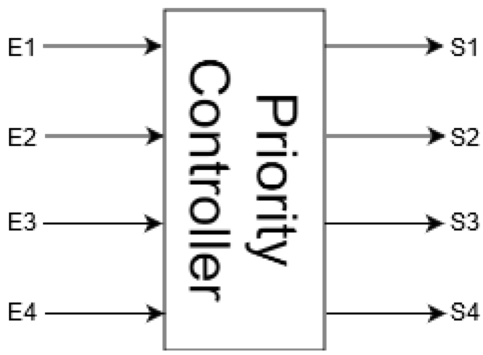
No more possible simplification.

Step 5 : Schematics



Priority controler :

Step 1 : Global Scheme



Step 2 : Truth Table

E1	E2	E3	E4	S1	S2	S3	S4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0

Or : (with reduction dashes)

E1	E2	E3	E4	S1	S2	S3	S4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	-	0	0	1	0
0	1	-	-	0	1	0	0
1	-	-	-	1	0	0	0

Step 3 : Canonical Disjunctive Functions

$$S1(E1,E2,E3,E4) = E1\cdot\overline{E2}\cdot\overline{E3}\cdot\overline{E4} + E1\cdot\overline{E2}\cdot\overline{E3}\cdot E4 + E1\cdot\overline{E2}\cdot E3\cdot\overline{E4} + E1\cdot\overline{E2}\cdot E3\cdot E4 + E1\cdot E2\cdot\overline{E3}\cdot\overline{E4} + E1\cdot E2\cdot\overline{E3}\cdot E4 + E1\cdot E2\cdot E3\cdot\overline{E4} + E1\cdot E2\cdot E3\cdot E4$$

$$S2(E1,E2,E3,E4) = \overline{E1}\cdot E2\cdot\overline{E3}\cdot\overline{E4} + \overline{E1}\cdot E2\cdot\overline{E3}\cdot E4 + \overline{E1}\cdot E2\cdot E3\cdot\overline{E4} + \overline{E1}\cdot E2\cdot E3\cdot E4$$

$$S3(E1,E2,E3,E4) = \overline{E1}\cdot\overline{E2}\cdot E3\cdot\overline{E4} + \overline{E1}\cdot\overline{E2}\cdot E3\cdot E4$$

$$S4(E1,E2,E3,E4) = \overline{E1}\cdot\overline{E2}\cdot\overline{E3}\cdot E4$$

Step 4 : Karnaugh Map

E3E4 \ E1E2	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

S1(E1,E2,E3,E4) = E3

E3E4 \ E1E2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	1	0	0
10	0	1	0	0

S2(E1,E2,E3,E4) = $\overline{E1}\cdot E2$

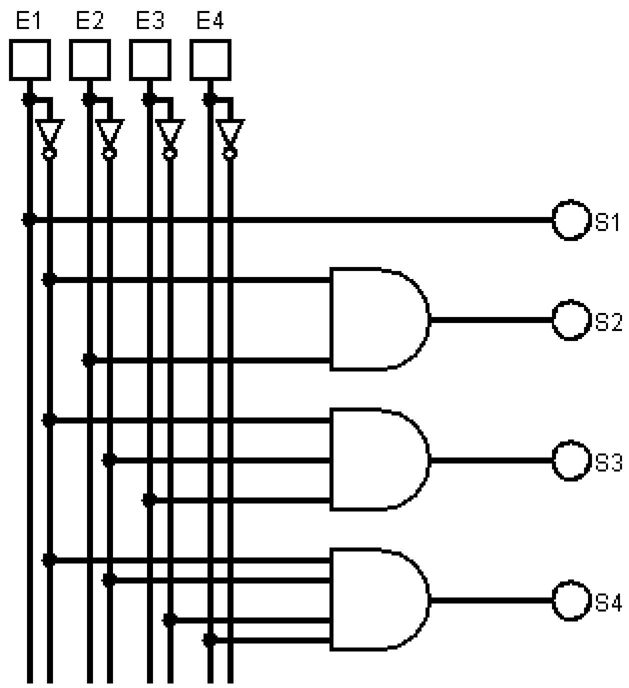
E3E4 \ E1E2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	0	0	0
10	1	0	0	0

S3(E1,E2,E3,E4) = $\overline{E1}\cdot\overline{E2}\cdot E3$

E3E4 \ E1E2	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	0	0	0	0
10	0	0	0	0

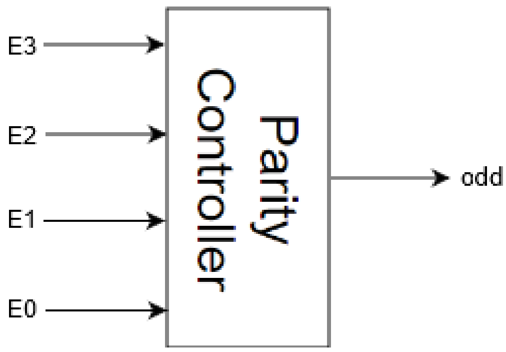
S4(E1,E2,E3,E4) = $\overline{E1}\cdot\overline{E2}\cdot\overline{E3}\cdot E4$

Step 5 : Schematics



Parity Controler :

Step 1 : Global Scheme



Step 2 : Truth Table

E3	E2	E1	E0	Odd
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Step 3 : Canonical Disjunctive Functions

$$Odd(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot E0 + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0}$$

Step 4 : Karnaugh Map

E1E0 \ E3E2	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$Odd(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot E0 +$
$E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0}$

No simplification done by Karnaugh map.

Algebraic Simplification

$Odd(E3,E2,E1,E0) = (\overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0}) + (\overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot E0) +$
$(E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0) + (E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0})$

$= \overline{E3}\cdot\overline{E2}\cdot(\overline{E1}\cdot E0 + E1\cdot\overline{E0}) + \overline{E3}\cdot E2\cdot(\overline{E1}\cdot\overline{E0} + E1\cdot E0) +$
$E3\cdot\overline{E2}\cdot(\overline{E1}\cdot\overline{E0} + E1\cdot E0) + E3\cdot E2\cdot(\overline{E1}\cdot E0 + E1\cdot\overline{E0})$

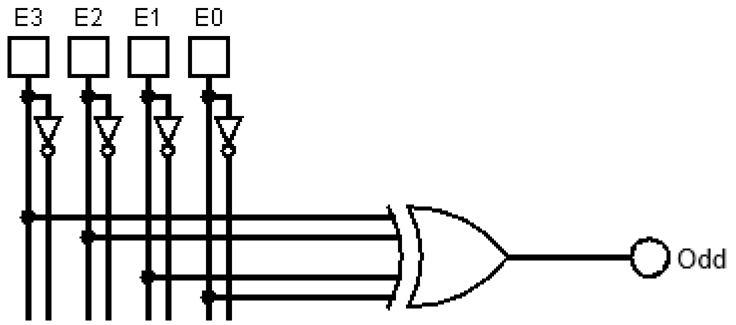
$= \overline{E3}\cdot\overline{E2}\cdot(E1 \oplus E0) + \overline{E3}\cdot E2\cdot(E1 \otimes E0) +$
$E3\cdot\overline{E2}\cdot(E1 \otimes E0) + E3\cdot E2\cdot(E1 \oplus E0)$

$= (\overline{E3}\cdot\overline{E2} + E3\cdot E2)\cdot(E1 \oplus E0) + (\overline{E3}\cdot E2 + E3\cdot\overline{E2})\cdot(E1 \otimes E0)$

$= (E3 \otimes E2)\cdot(E1 \oplus E0) + (E3 \oplus E2)\cdot(E1 \otimes E0)$

We put $(X = E1 \oplus E0)$ and $(Y = E3 \oplus E2)$
$= \overline{Y}\cdot X + Y\cdot\overline{X} = Y \oplus X = E3 \oplus E2 \oplus E1 \oplus E0$

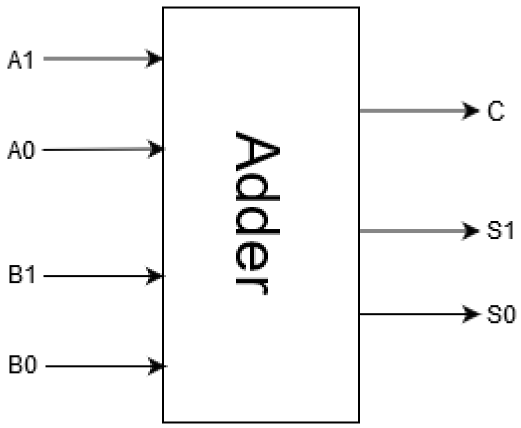
Step 5 : Schematics



Remark : The technic of using XOR or XNOR to implement the Parity Controler is a well known method in Hardware design domain.

Adder :

Step 1 : Global Scheme



Step 2 : Truth Table

A1	A0	B1	B0	S1	S0	C
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	0	1	1	0	1	1
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Step 3 : Canonical Disjunctive Functions

$$S1(A1,A0,B1,B0) = \overline{A1}\cdot\overline{A0}\cdot B1\cdot\overline{B0} + \overline{A1}\cdot\overline{A0}\cdot B1\cdot B0 + \overline{A1}\cdot A0\cdot\overline{B1}\cdot B0 + \overline{A1}\cdot A0\cdot B1\cdot\overline{B0} + A1\cdot\overline{A0}\cdot\overline{B1}\cdot\overline{B0} + A1\cdot\overline{A0}\cdot\overline{B1}\cdot B0 + A1\cdot A0\cdot\overline{B1}\cdot\overline{B0} + A1\cdot A0\cdot B1\cdot B0$$

$$S0(A1,A0,B1,B0) = \overline{A1}\cdot\overline{A0}\cdot\overline{B1}\cdot B0 + \overline{A1}\cdot\overline{A0}\cdot B1\cdot B0 + \overline{A1}\cdot A0\cdot\overline{B1}\cdot\overline{B0} + \overline{A1}\cdot A0\cdot B1\cdot\overline{B0} + A1\cdot\overline{A0}\cdot\overline{B1}\cdot B0 + A1\cdot\overline{A0}\cdot B1\cdot B0 + A1\cdot A0\cdot\overline{B1}\cdot\overline{B0} + A1\cdot A0\cdot B1\cdot\overline{B0}$$

$$C(A1,A0,B1,B0) = \overline{A1}\cdot A0\cdot B1\cdot B0 + A1\cdot\overline{A0}\cdot B1\cdot\overline{B0} + A1\cdot\overline{A0}\cdot B1\cdot B0 + A1\cdot A0\cdot\overline{B1}\cdot B0 + A1\cdot A0\cdot B1\cdot\overline{B0} + A1\cdot A0\cdot B1\cdot B0$$

Step 4 : Karnaugh Map

B1B0 \ A1A0	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	1	0	1	0
10	1	1	0	0

$$S1(A1,A0,B1,B0) = \overline{A1}\cdot\overline{A0}\cdot B1 + \overline{A1}\cdot B1\cdot\overline{B0} + \overline{A1}\cdot A0\cdot\overline{B1}\cdot B0 + A1\cdot A0\cdot B1\cdot B0 + A1\cdot\overline{B1}\cdot\overline{B0} + A1\cdot\overline{A0}\cdot\overline{B1}$$

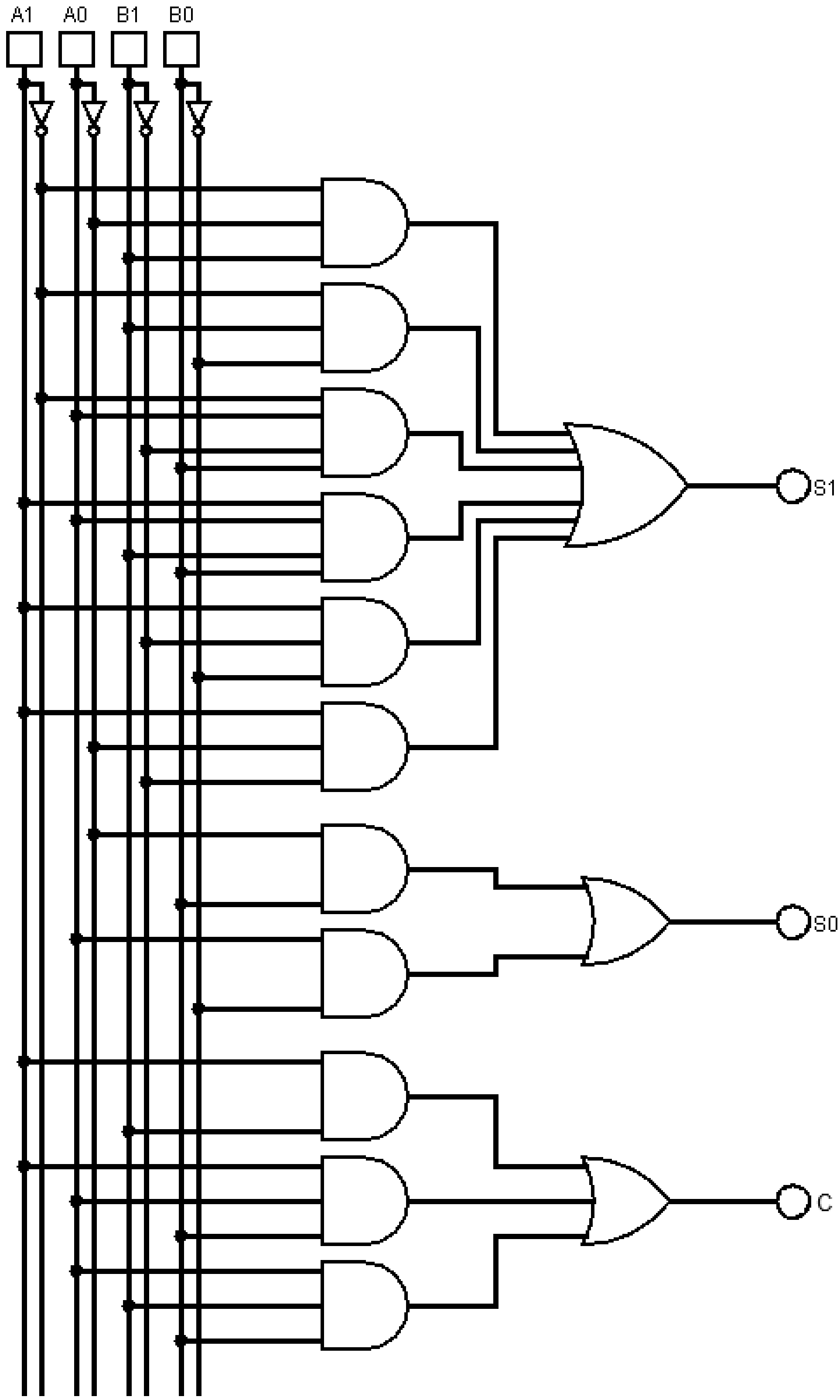
B1B0 \ A1A0	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	0	1
10	0	1	1	0

$$S0(A1,A0,B1,B0) = \overline{A0}\cdot B0 + A0\cdot\overline{B0}$$

B1B0 \ A1A0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	1	1	1
10	0	0	1	1

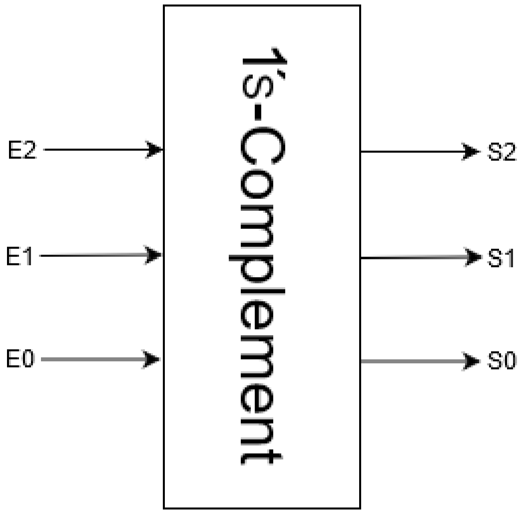
$$C(A1,A0,B1,B0) = A1\cdot B1 + A1\cdot A0\cdot B0 + A0\cdot B1\cdot B0$$

Step 5 : Schematics



1s-Complement :

<u>Step 1</u> : Global Scheme



<u>Step 2</u> : Truth Table

E2	E1	E0	S2	S1	S0
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

<u>Step 3</u> : Canonical Disjunctive Functions

$S2(E2,E1,E0) = \overline{E2}\cdot\overline{E1}\cdot\overline{E0} + \overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E2}\cdot E1\cdot\overline{E0} + \overline{E2}\cdot E1\cdot E0$

$S1(E2,E1,E0) = \overline{E2}\cdot\overline{E1}\cdot\overline{E0} + \overline{E2}\cdot\overline{E1}\cdot E0 + E2\cdot\overline{E1}\cdot\overline{E0} + E2\cdot\overline{E1}\cdot E0$

$S0(E2,E1,E0) = \overline{E2}\cdot\overline{E1}\cdot\overline{E0} + \overline{E2}\cdot E1\cdot\overline{E0} + E2\cdot\overline{E1}\cdot\overline{E0} + E2\cdot E1\cdot\overline{E0}$

Step 4 : Karnaugh Map

E0 \ E2E1	00	01	11	10
0	1	1	0	0
1	1	1	0	0

S2(E2,E1,E0) = $\overline{E2}$

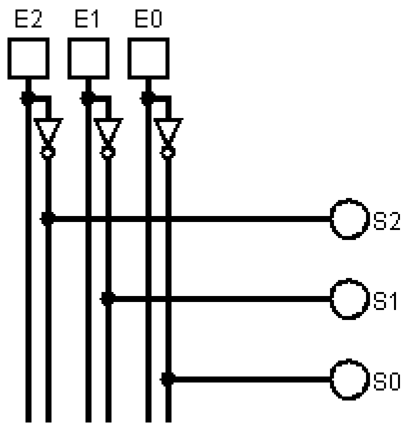
E0 \ E2E1	00	01	11	10
0	1	0	0	1
1	1	0	0	1

S1(E2,E1,E0) = $\overline{E1}$

E0 \ E2E1	00	01	11	10
0	1	1	1	1
1	0	0	0	0

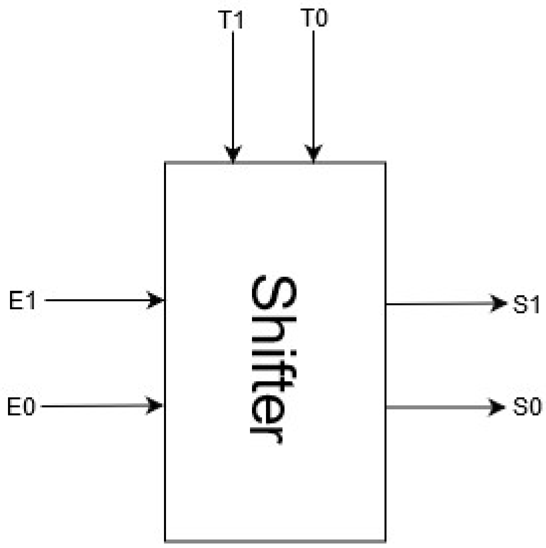
S0(E2,E1,E0) = $\overline{E0}$

Step 5 : Schematics



Shifter :

Step 1 : Global Scheme



Step 2 : Truth Table

T1	T0	E1	E0	S1	S0
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	-	-
1	1	0	1	-	-
1	1	1	0	-	-
1	1	1	1	-	-

<u>Step 3</u> : Canonical Disjunctive Functions

$S1(T1,T0,E1,E0) = \overline{T1}\cdot\overline{T0}\cdot E1\cdot\overline{E0} + \overline{T1}\cdot\overline{T0}\cdot E1\cdot E0 + \overline{T1}\cdot T0\cdot\overline{E1}\cdot E0 + \overline{T1}\cdot T0\cdot E1\cdot E0$

$S0(T1,T0,E1,E0) = \overline{T1}\cdot\overline{T0}\cdot\overline{E1}\cdot E0 + \overline{T1}\cdot\overline{T0}\cdot E1\cdot E0$

<u>Step 4</u> : Karnaugh Map

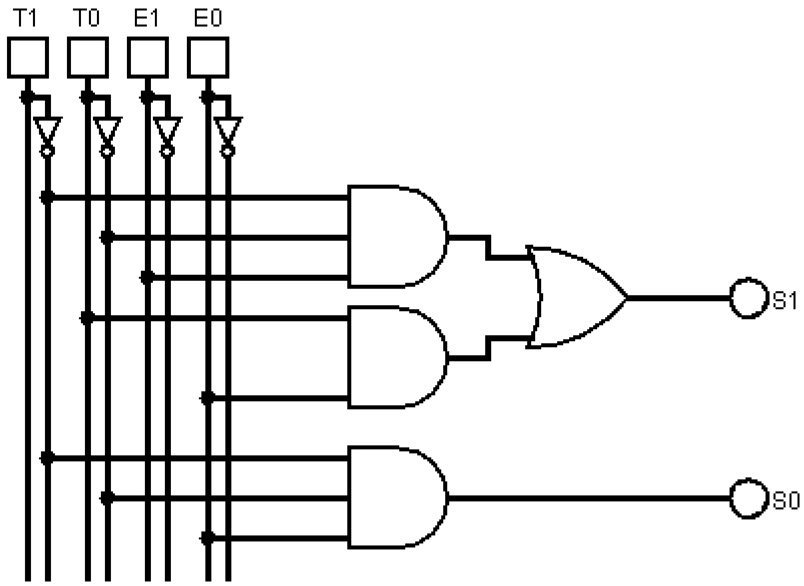
E1E0 \ T1T0	00	01	11	10
00	0	0	-	0
01	0	1	-	0
11	1	1	-	0
10	1	0	-	0

E1E0 \ T1T0	00	01	11	10
00	0	0	-	0
01	1	0	-	0
11	1	0	-	0
10	0	0	-	0

$S1(T1,T0,E1,E0) = \overline{T1}\cdot\overline{T0}\cdot E1 + T0\cdot E0$

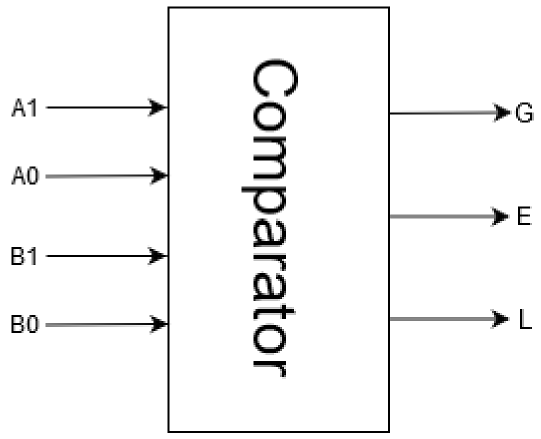
$S0(T1,T0,E1,E0) = \overline{T1}\cdot\overline{T0}\cdot E0$

<u>Step 5</u> : Schematics



Comparator :

Step 1 : Global Scheme



Step 2 : Truth Table

A1	A0	B1	B0	G	E	L
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Step 3 : Canonical Disjunctive Functions

$$G(A1,A0,B1,B0) = \overline{A1}\cdot A0\cdot \overline{B1}\cdot \overline{B0} + A1\cdot \overline{A0}\cdot \overline{B1}\cdot \overline{B0} + A1\cdot \overline{A0}\cdot \overline{B1}\cdot B0 + A1\cdot A0\cdot \overline{B1}\cdot \overline{B0} + A1\cdot A0\cdot \overline{B1}\cdot B0 + A1\cdot A0\cdot B1\cdot \overline{B0}$$

$$E(A1,A0,B1,B0) = \overline{A1}\cdot \overline{A0}\cdot \overline{B1}\cdot \overline{B0} + \overline{A1}\cdot A0\cdot \overline{B1}\cdot B0 + A1\cdot \overline{A0}\cdot B1\cdot \overline{B0} + A1\cdot A0\cdot B1\cdot B0$$

$$L(A1,A0,B1,B0) = \overline{A1}\cdot \overline{A0}\cdot \overline{B1}\cdot B0 + \overline{A1}\cdot \overline{A0}\cdot B1\cdot \overline{B0} + \overline{A1}\cdot \overline{A0}\cdot B1\cdot B0 + \overline{A1}\cdot A0\cdot B1\cdot \overline{B0} + \overline{A1}\cdot A0\cdot B1\cdot B0 + A1\cdot \overline{A0}\cdot B1\cdot B0$$

Step 4 : Karnaugh Map

B1B0 \ A1A0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$$G(A1,A0,B1,B0) = A1\cdot \overline{B1} + A0\cdot \overline{B1}\cdot \overline{B0} + A1\cdot A0\cdot \overline{B0}$$

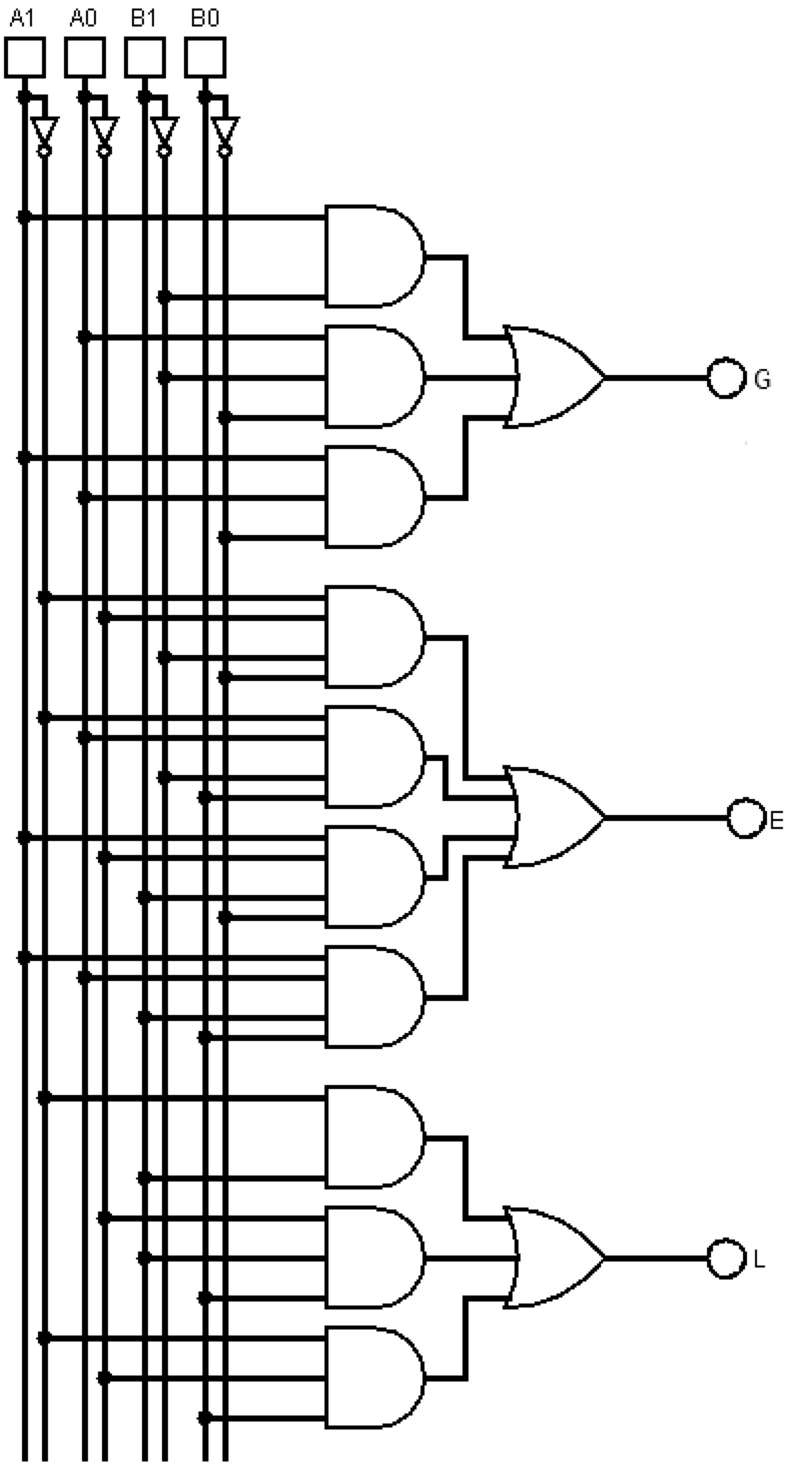
B1B0 \ A1A0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$$E(A1,A0,B1,B0) = \overline{A1}\cdot \overline{A0}\cdot \overline{B1}\cdot \overline{B0} + \overline{A1}\cdot A0\cdot \overline{B1}\cdot B0 + A1\cdot \overline{A0}\cdot B1\cdot \overline{B0} + A1\cdot A0\cdot B1\cdot B0$$

B1B0 \ A1A0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

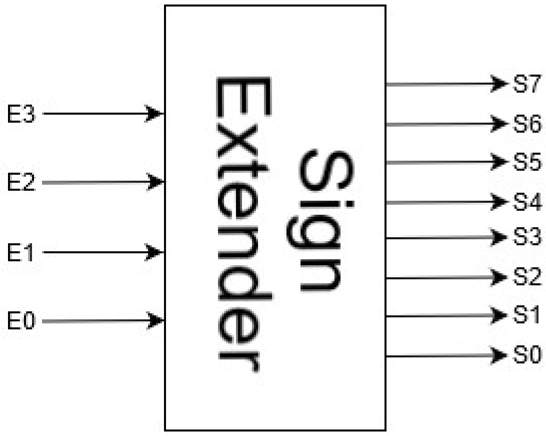
$$L(A1,A0,B1,B0) = \overline{A1}\cdot B1 + \overline{A0}\cdot B1\cdot B0 + \overline{A1}\cdot \overline{A0}\cdot B0$$

Step 5 : Schematics



Signe Extender :

Step 1 : Global Scheme



Step 2 : Truth Table

E3	E2	E1	E0	S7	S6	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	0	0
0	1	0	1	0	0	0	0	0	1	0	1
0	1	1	0	0	0	0	0	0	1	1	0
0	1	1	1	0	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	0	0	0
1	0	0	1	1	1	1	1	1	0	0	1
1	0	1	0	1	1	1	1	1	0	1	0
1	0	1	1	1	1	1	1	1	0	1	1
1	1	0	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1

Step 3 : Canonical Disjunctive Functions

$$S7(E3,E2,E1,E0) = E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + E3\cdot\overline{E2}\cdot E1\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot\overline{E0} + E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0} + E3\cdot E2\cdot E1\cdot E0$$

$$S6(E3,E2,E1,E0) = S5(E3,E2,E1,E0) = S4(E3,E2,E1,E0) = S3(E3,E2,E1,E0) = S7(E3,E2,E1,E0)$$

$$S2(E3,E2,E1,E0) = \overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot E2\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot E2\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot\overline{E0} + E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0} + E3\cdot E2\cdot E1\cdot E0$$

$$S1(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot\overline{E2}\cdot E1\cdot E0 + \overline{E3}\cdot E2\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot E1\cdot E0 + E3\cdot\overline{E2}\cdot E1\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot E1\cdot\overline{E0} + E3\cdot E2\cdot E1\cdot E0$$

$$S0(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot E0 + \overline{E3}\cdot E2\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot E2\cdot E1\cdot E0 + E3\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot E2\cdot E1\cdot E0$$

Step 4 : Karnaugh Map

E1E0 \ E3E2	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	1	1
10	0	0	1	1

S7(E3,E2,E1,E0) = E3

E1E0 \ E3E2	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

S2(E3,E2,E1,E0) = E2

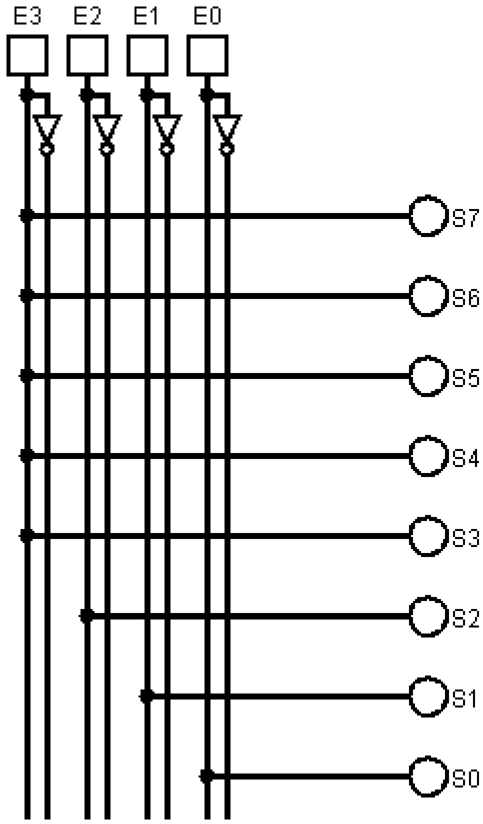
E1E0 \ E3E2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

S1(E3,E2,E1,E0) = E1

E1E0 \ E3E2	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

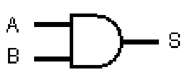
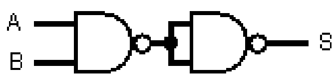
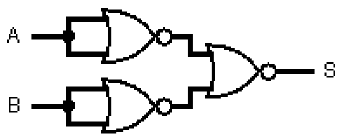
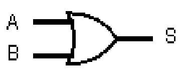
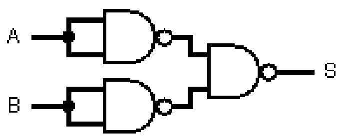
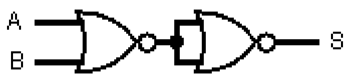
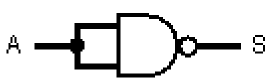
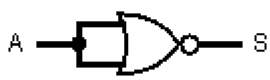
S0(E3,E2,E1,E0) = E0

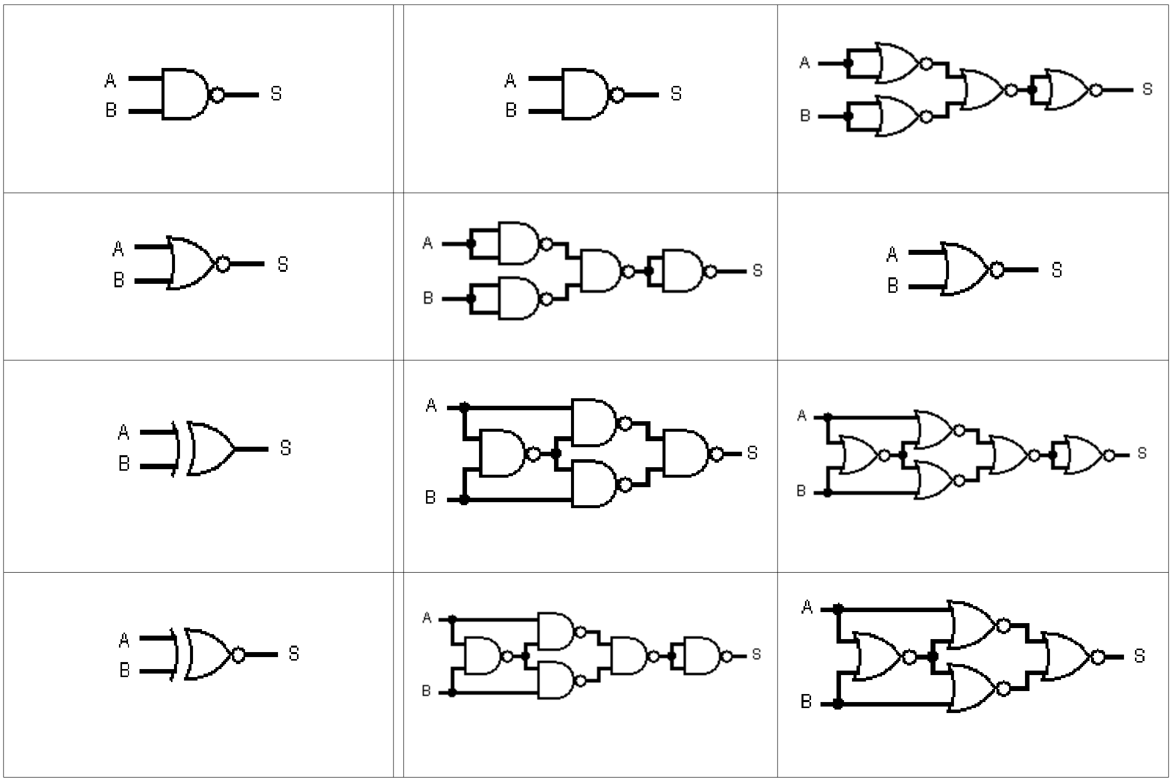
Step 5 : Schematics



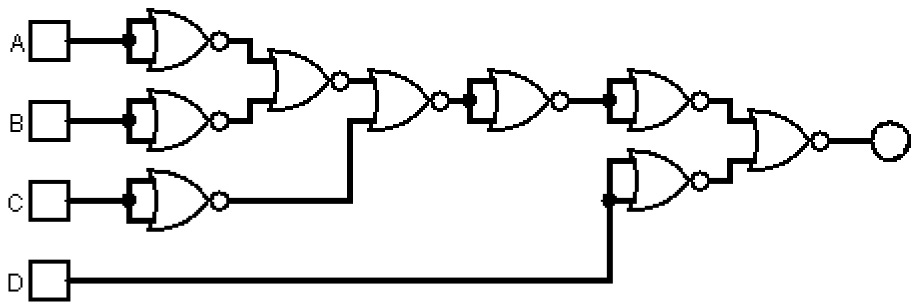
Exercise 04 :

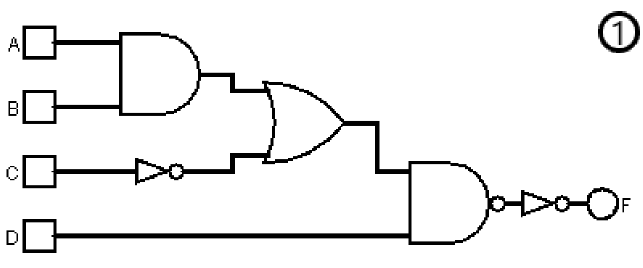
1)

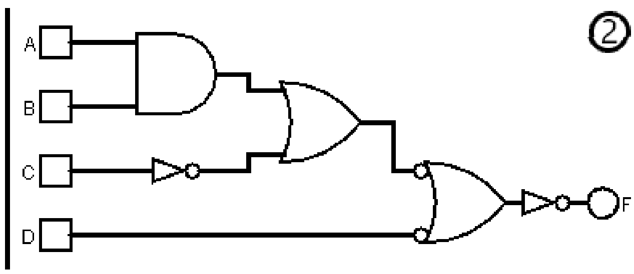
Porte logique	Portes NAND	Portes NOR
		
		
		

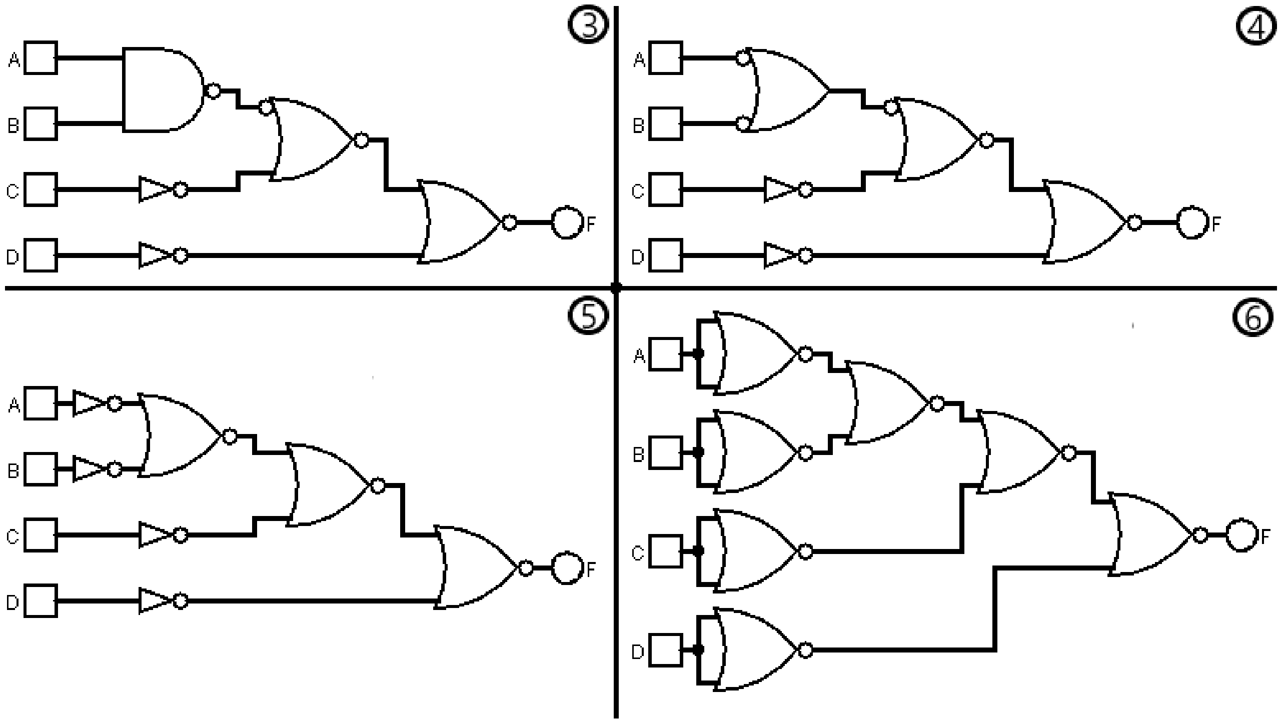


2)

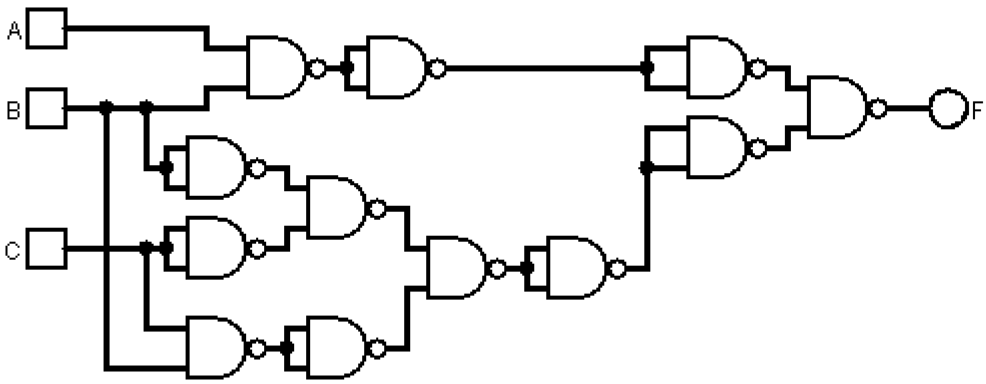


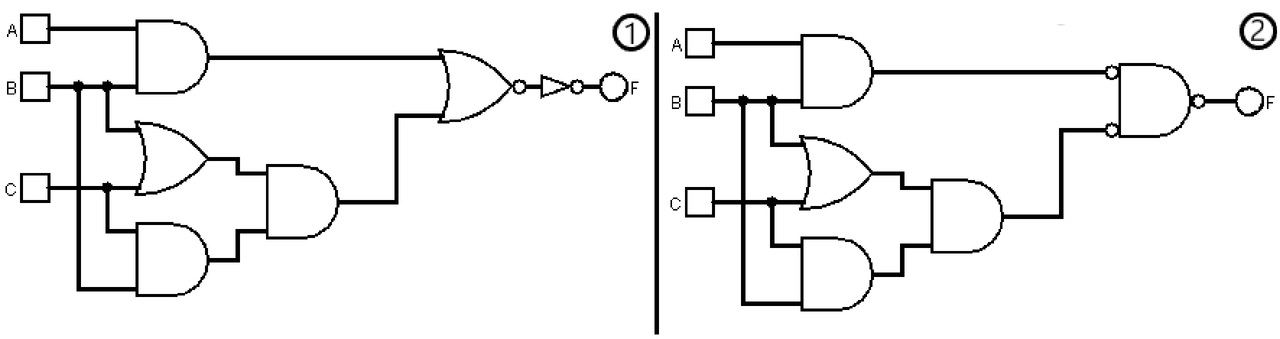


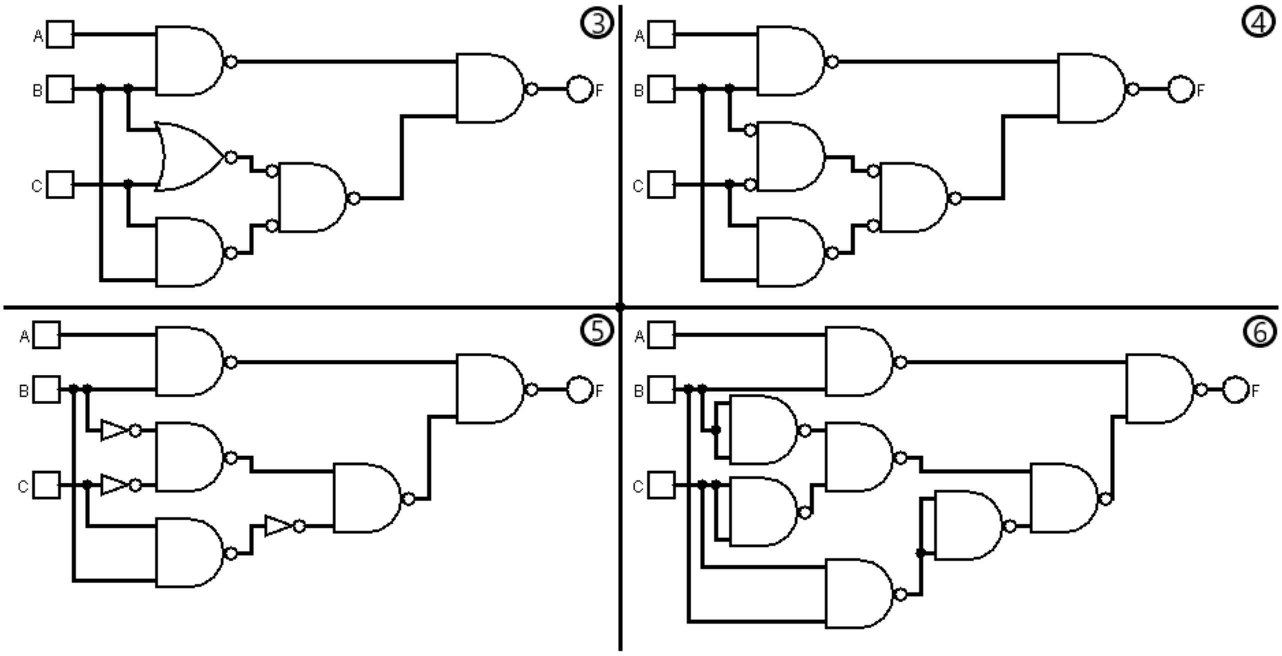




3)





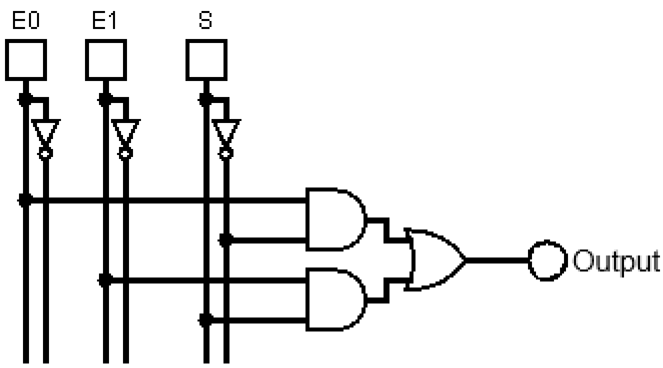


4) The conclusion about the difference between using the gate-by-gate replacement method, and the bubble push method, is that the latter reduces the number of gates more than the former.

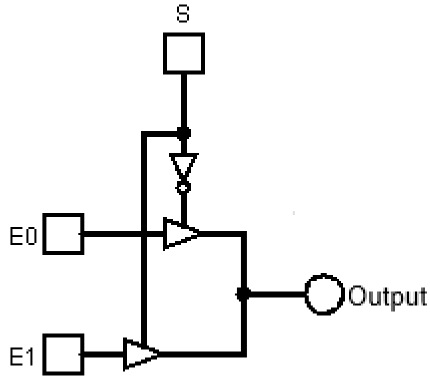
Exercise 05 :

1) The construction of the 2-input Multiplexer with the 5-step method:

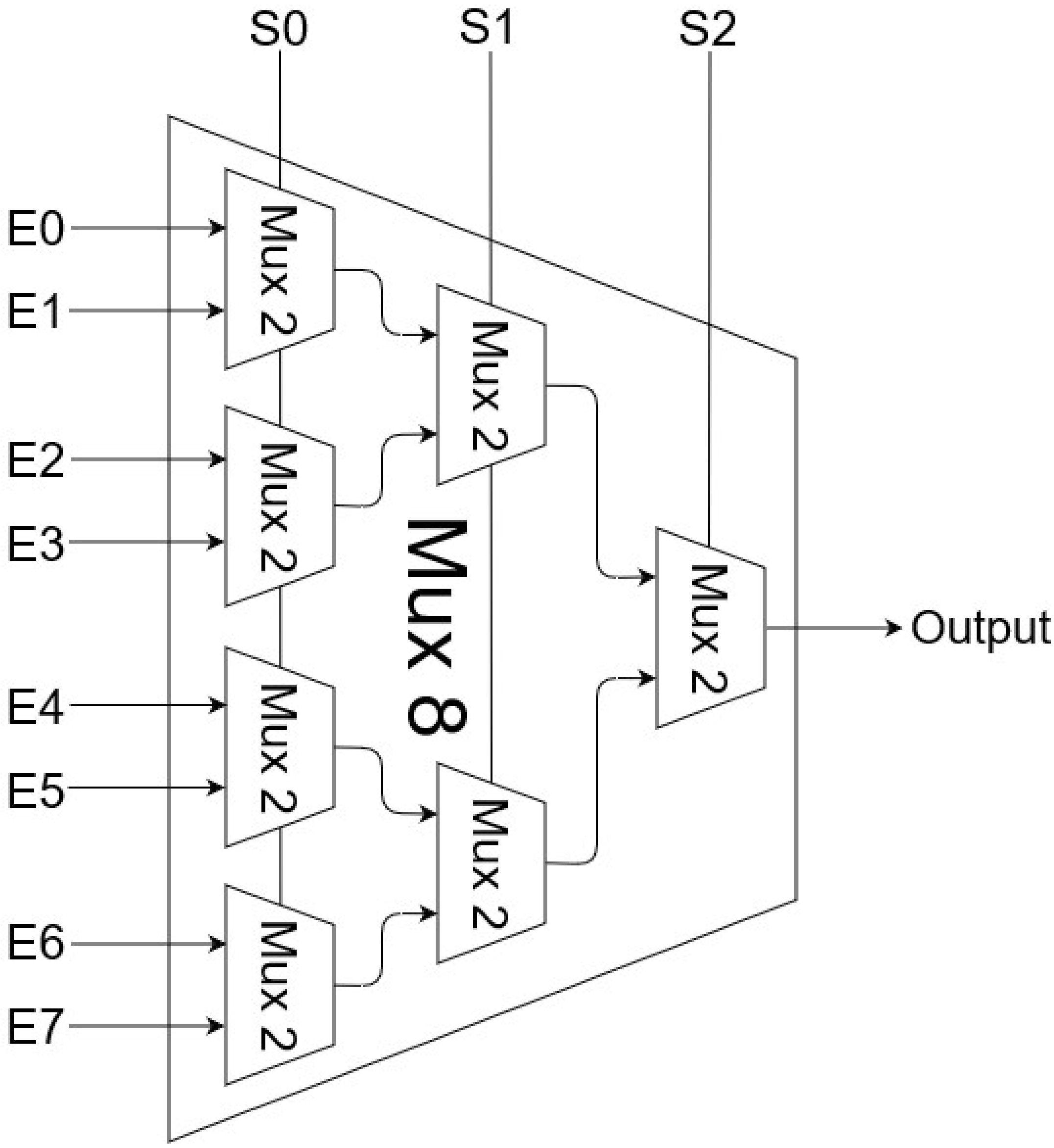
Previously done in exercise 3



The construction of the 2-input Multiplexer using Tristate Buffers :

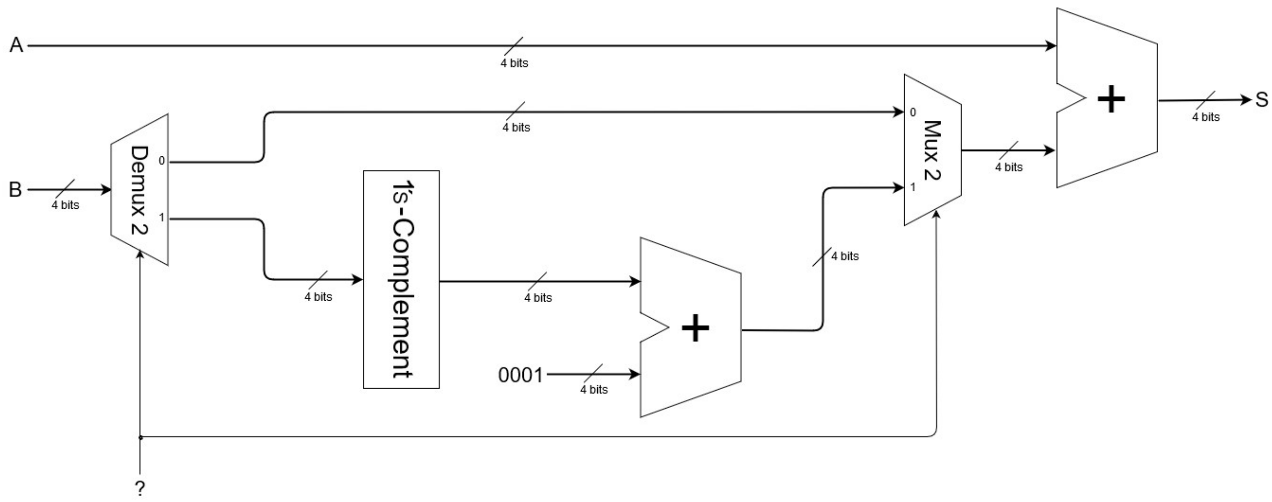


The construction of the 8-input Multiplexer using the 2-input Multiplexers :



2) Description of the circuit :

The circuit in global has 2 inputs A and B. A arrives directly at the final adder while B has the possibility of taking 2 different paths chosen by the Multiplexer and the Demultiplexer. Input B has a direct path and a sencond which must pass by the 1's-Complement followed by an addition +1. In the circuit we can observe the control of data flow exercised by the Multiplexer/Demultiplexer to choose a given path. It is the 3rd entry (?) that makes it possible to choose whether the flow of B must pass directly or go through the 1's-Complement path followed by the +1 adder.



Q : What does the circuit do?

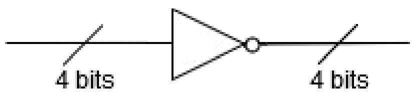
A : This circuit do the addition and subtraction in 2's-Complement. Subtraction is done by making negative the second operand by applying 1's-Complement followed by the addition +1 (ex: 1-2 becomes 1+(-2), -2 is the 2's Complement of 2).

Q : Give a name for the 3rd entry (in ?)

A : The appropriate name is *$\overline{\text{addition}}$/subtraction*. If the input is at 0 the circuit does the addition (hence *$\overline{\text{addition}}$*), if it's 1 it does the subtraction. This way of naming pins is widely used in the Hardware design domain.

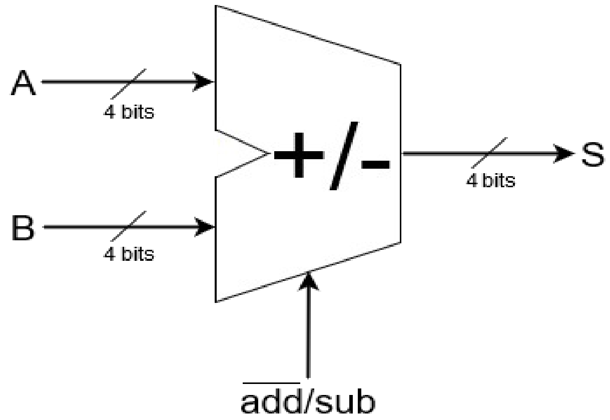
Q : Replace the 1's-Complement circuit with a simpler equivalent circuit.

A :



Q : Draw a Global scheme for the circuit.

R :

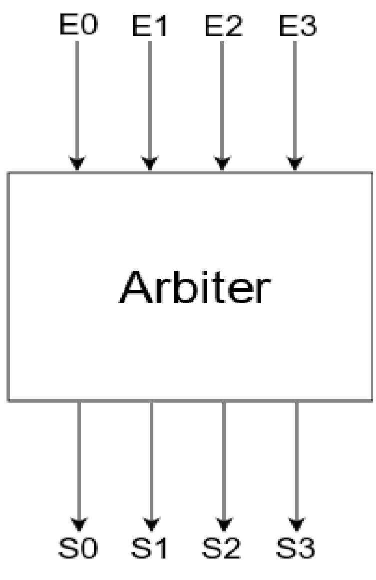


Remark 1: The purpose of the previous circuit was to demonstrate the way in which the Multiplexer/Demultiplexer achieve flow control, however this is not the best way to implement the Adder/Subtractor circuit, other more optimal constructions will be studied in the next exercise.

Remark 2: In the question where it was necessary to replace 1's-Complement a simpler equivalent circuit, the NOT gate with 4 inputs and 4 outputs is interpreted as 4 NOT gates with a single input and a single output put altogether in parallel. But if it was an AND gate for example, it could cause confusion between; 4 gates in parallel for each input or just one with 4 inputs put into logic (E0·E1·E2·E3). The 2 interpretations are correct and there is no precise rule to distinguish them, generally it is necessary to distinguish the context (the role) of its use in the circuit.

3) The Arbiter circuit construction :

<u>Step 1</u> : Global Scheme



By observation we can think of subdividing the combinational circuit into 2 separate simpler combinational circuits, this makes the construction easier.

Step 2 : Truth Table

E0	E1	S0	S1
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

E2	E3	S2	S3
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Step 3 : Canonical Disjunctive Functions

$S0(E0,E1) = E0 \cdot \overline{E1} + E0 \cdot E1$
$S1(E0,E1) = \overline{E0} \cdot E1 + E0 \cdot E1$

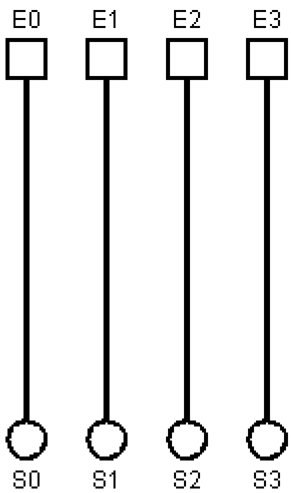
$S2(E2,E3) = E2 \cdot \overline{E3} + E2 \cdot E3$
$S3(E2,E3) = \overline{E2} \cdot E3 + E2 \cdot E3$

Step 4 : By observation

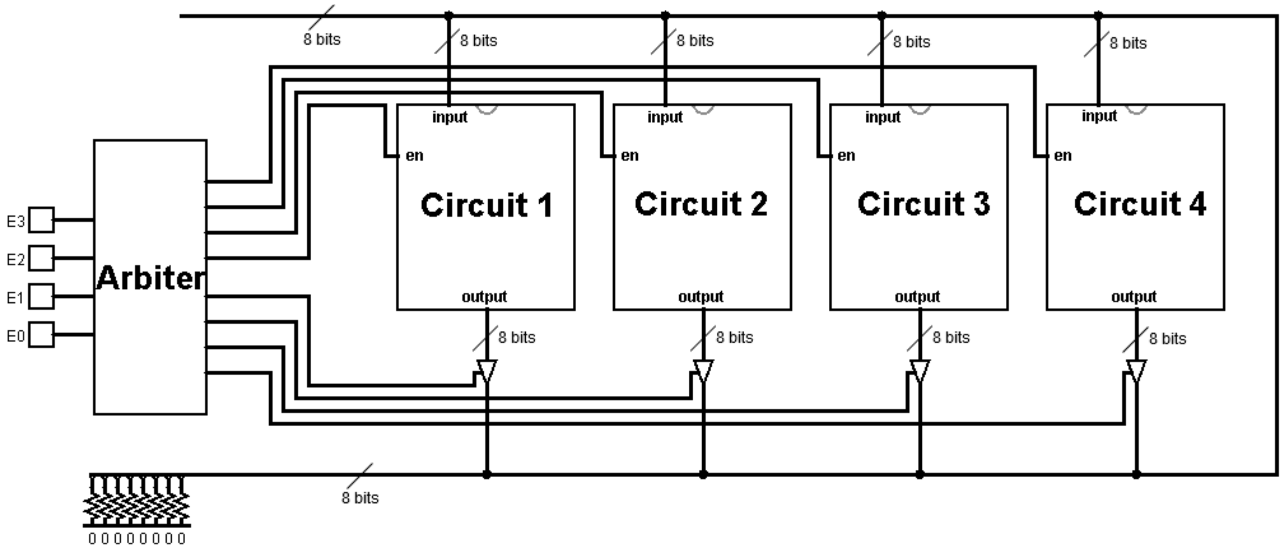
S0(E0,E1) = E0
S1(E0,E1) = E1

S2(E2,E3) = E2
S3(E2,E3) = E3

Step 5 : Schematics

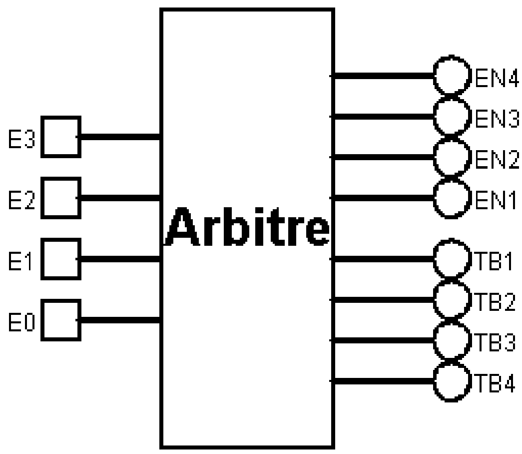


4) The micro-architecture construction :



The Arbitrator circuit Construction :

<u>Step 1</u> : Global Scheme



E2,E1,E0	Departure	Arrival
000	Circuit 1	Circuit 2
001	Circuit 1	Circuit 3
010	Circuit 1	Circuit 4
011	Circuit 2	Circuit 3
100	Circuit 2	Circuit 4
101	Circuit 3	Circuit 4

110 et 111 : not used.
E3 is the oriontation : 0 same way, 1 opposite way.

Step 2 : Truth Table

E3	E2	E1	E0	EN1	EN2	EN3	EN4	TB1	TB2	TB3	TB4
0	0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	1	0	1	0	0	0
0	0	1	0	0	0	0	1	1	0	0	0
0	0	1	1	0	0	1	0	0	1	0	0
0	1	0	0	0	0	0	1	0	1	0	0
0	1	0	1	0	0	0	1	0	0	1	0
0	1	1	0	-	-	-	-	-	-	-	-
0	1	1	1	-	-	-	-	-	-	-	-
1	0	0	0	1	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	1	0
1	0	1	0	1	0	0	0	0	0	0	1
1	0	1	1	0	1	0	0	0	0	1	0
1	1	0	0	0	1	0	0	0	0	0	1
1	1	0	1	0	0	1	0	0	0	0	1
1	1	1	0	-	-	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-	-	-

Step 3 : Canonical Disjunctive Functions

EN1(E3,E2,E1,E0) = $E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + E3\cdot\overline{E2}\cdot E1\cdot\overline{E0}$

EN2(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot\overline{E0}$

EN3(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E1}\cdot E0$

EN4(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot E2\cdot\overline{E1}\cdot E0$

TB1(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + \overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + \overline{E3}\cdot\overline{E2}\cdot E1\cdot\overline{E0}$

TB2(E3,E2,E1,E0) = $\overline{E3}\cdot\overline{E2}\cdot E1\cdot E0 + \overline{E3}\cdot E2\cdot\overline{E1}\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0}$

TB3(E3,E2,E1,E0) = $\overline{E3}\cdot E2\cdot\overline{E1}\cdot E0 + E3\cdot\overline{E2}\cdot\overline{E1}\cdot E0 + E3\cdot\overline{E2}\cdot E1\cdot E0$

TB4(E3,E2,E1,E0) = $E3\cdot\overline{E2}\cdot E1\cdot\overline{E0} + E3\cdot E2\cdot\overline{E1}\cdot\overline{E0} + E3\cdot E2\cdot\overline{E1}\cdot E0$

Step 4 : Karnaugh Map

E1E0 \ E3E2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	-	-	0
10	0	-	-	1

E1E0 \ E3E2	00	01	11	10
00	1	0	1	0
01	0	0	0	0
11	0	-	-	1
10	0	-	-	0

EN1(E3,E2,E1,E0) = $E3\cdot\overline{E2}\cdot\overline{E1} + E3\cdot E1\cdot\overline{E0}$

EN2(E3,E2,E1,E0)= $\overline{E3}\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0} + E3\cdot E1\cdot E0 + E3\cdot E2\cdot\overline{E0}$

E1E0 \ E3E2	00	01	11	10
00	0	0	0	0
01	1	0	1	0
11	1	-	-	0
10	0	-	-	0

$EN3(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot E0 + E3\cdot E2\cdot E0$

E1E0 \ E3E2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	-	-	0
10	1	-	-	0

$EN4(E3,E2,E1,E0) = \overline{E3}\cdot E1\cdot\overline{E0} + \overline{E3}\cdot E2$

E1E0 \ E3E2	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	0	-	-	0
10	1	-	-	0

$TB1(E3,E2,E1,E0) = \overline{E3}\cdot\overline{E2}\cdot\overline{E1} + \overline{E3}\cdot E1\cdot\overline{E0}$

E1E0 \ E3E2	00	01	11	10
00	0	1	0	1
01	0	0	0	0
11	1	-	-	0
10	0	-	-	0

$TB2(E3,E2,E1,E0) = \overline{E3}\cdot E1\cdot E0 + \overline{E3}\cdot E2\cdot\overline{E0} + E3\cdot\overline{E2}\cdot\overline{E1}\cdot\overline{E0}$

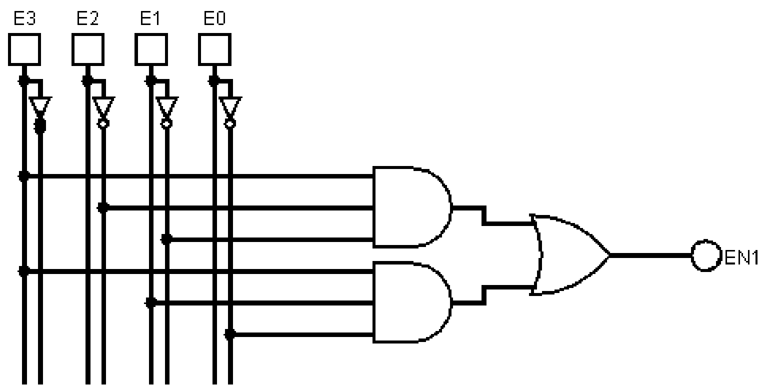
E1E0 \ E3E2	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	0	-	-	1
10	0	-	-	0

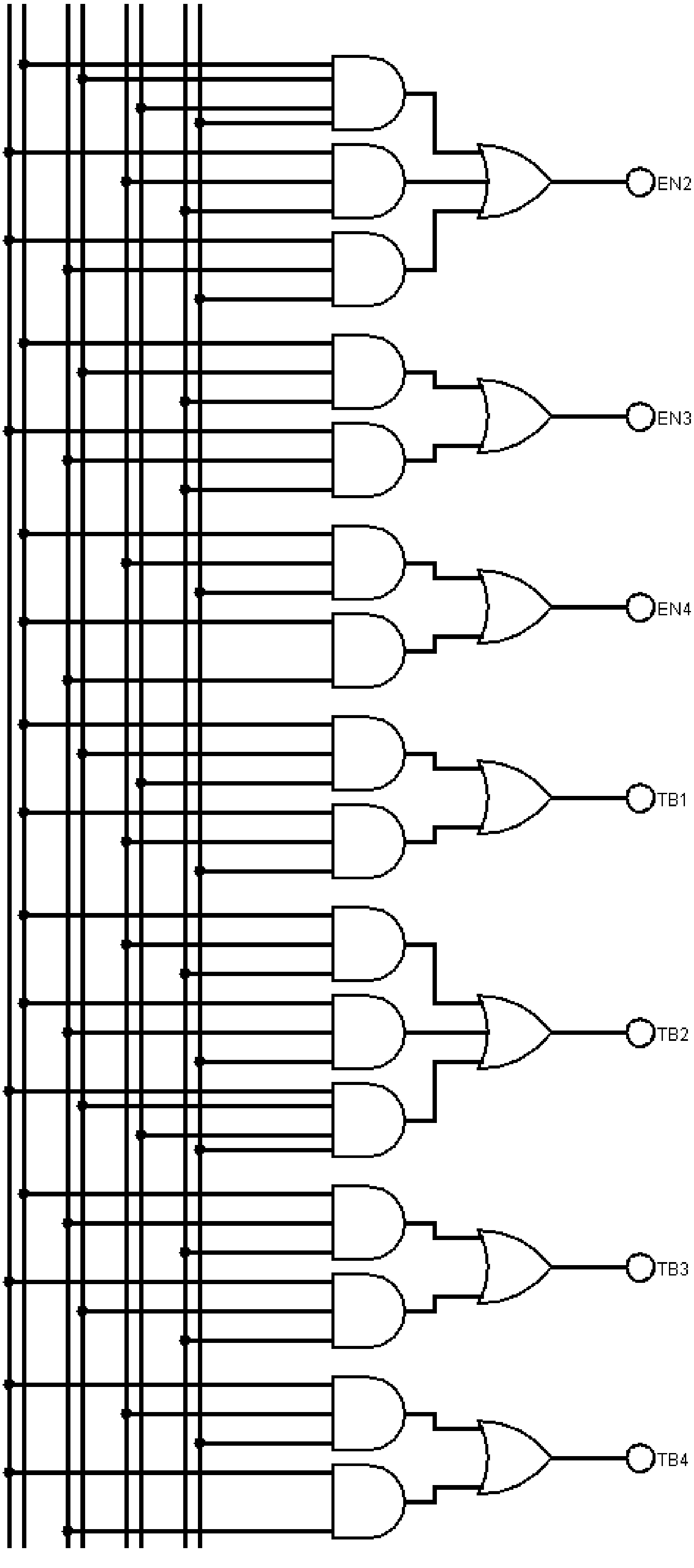
$TB3(E3,E2,E1,E0) = \overline{E3}\cdot E2\cdot E0 + E3\cdot\overline{E2}\cdot E0$

E1E0 \ E3E2	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	-	-	0
10	0	-	-	1

$TB4(E3,E2,E1,E0) = E3\cdot E1\cdot\overline{E0} + E3\cdot E2$

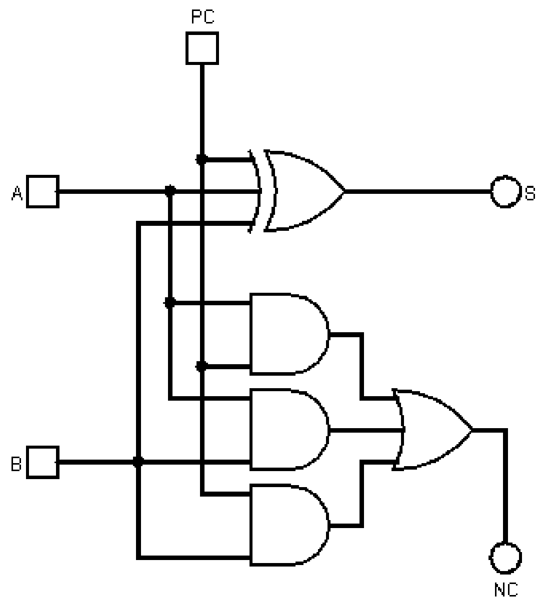
<u>Step 5</u> : Schematics



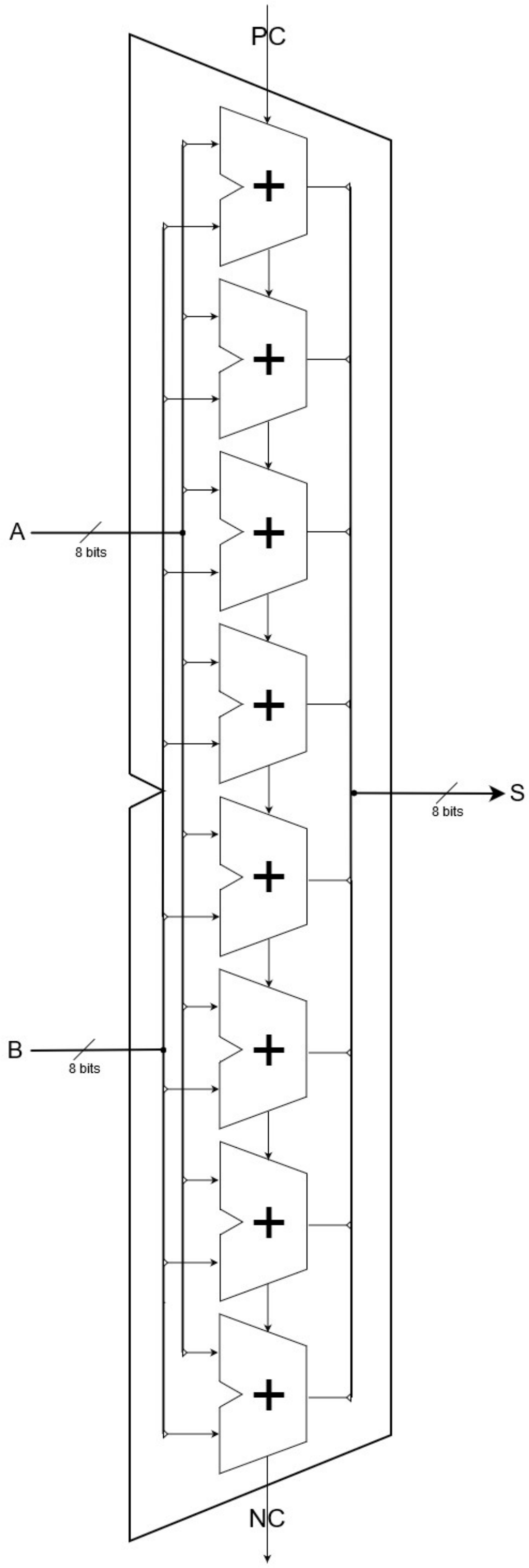

EN2
EN3
EN4
TB1
TB2
TB3
TB4

Exercise 06 :

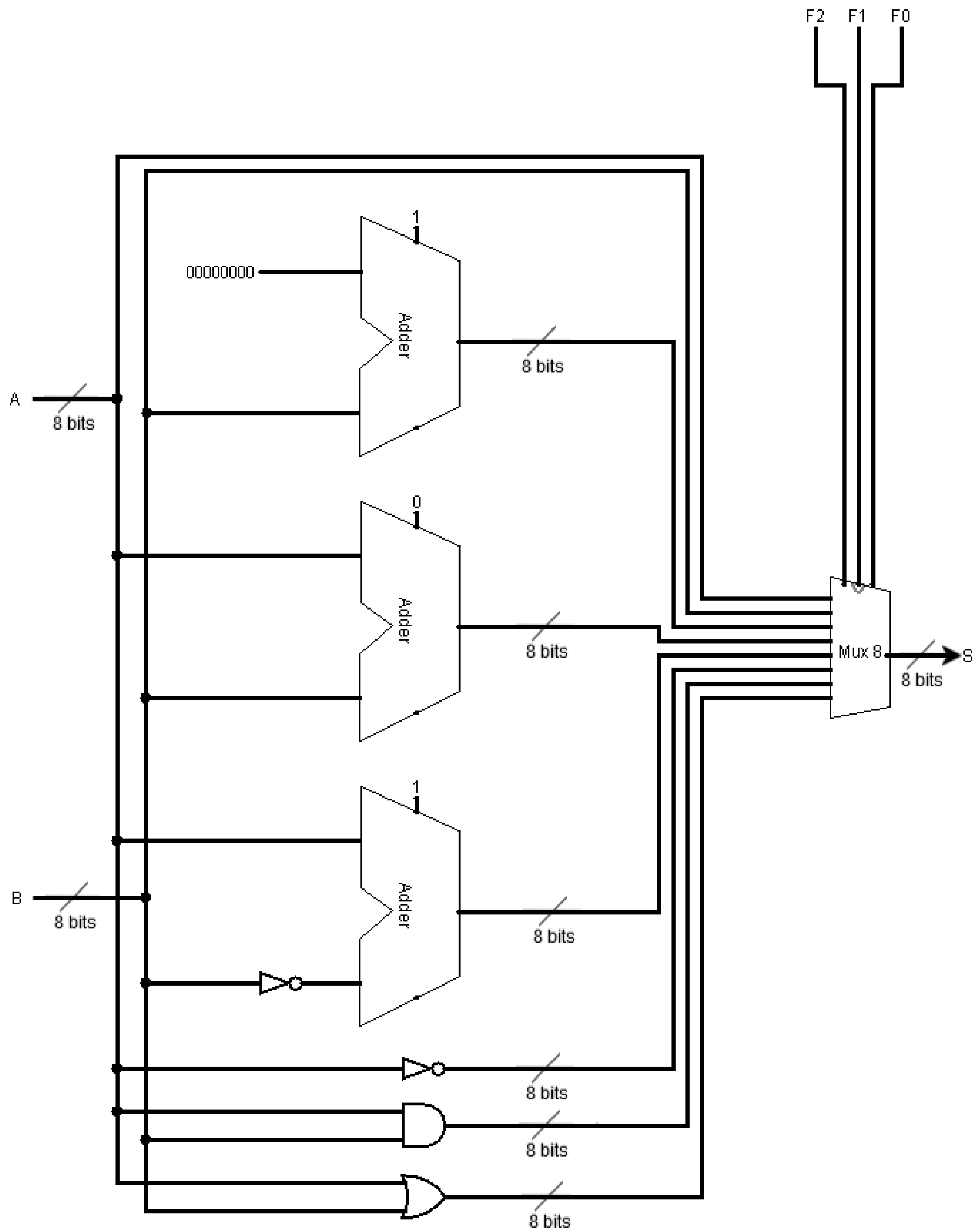
1) To do the addition we will use the slicing of Full-Adders (check the lecture), this will simplify the B+1 operation.



Full-Adder

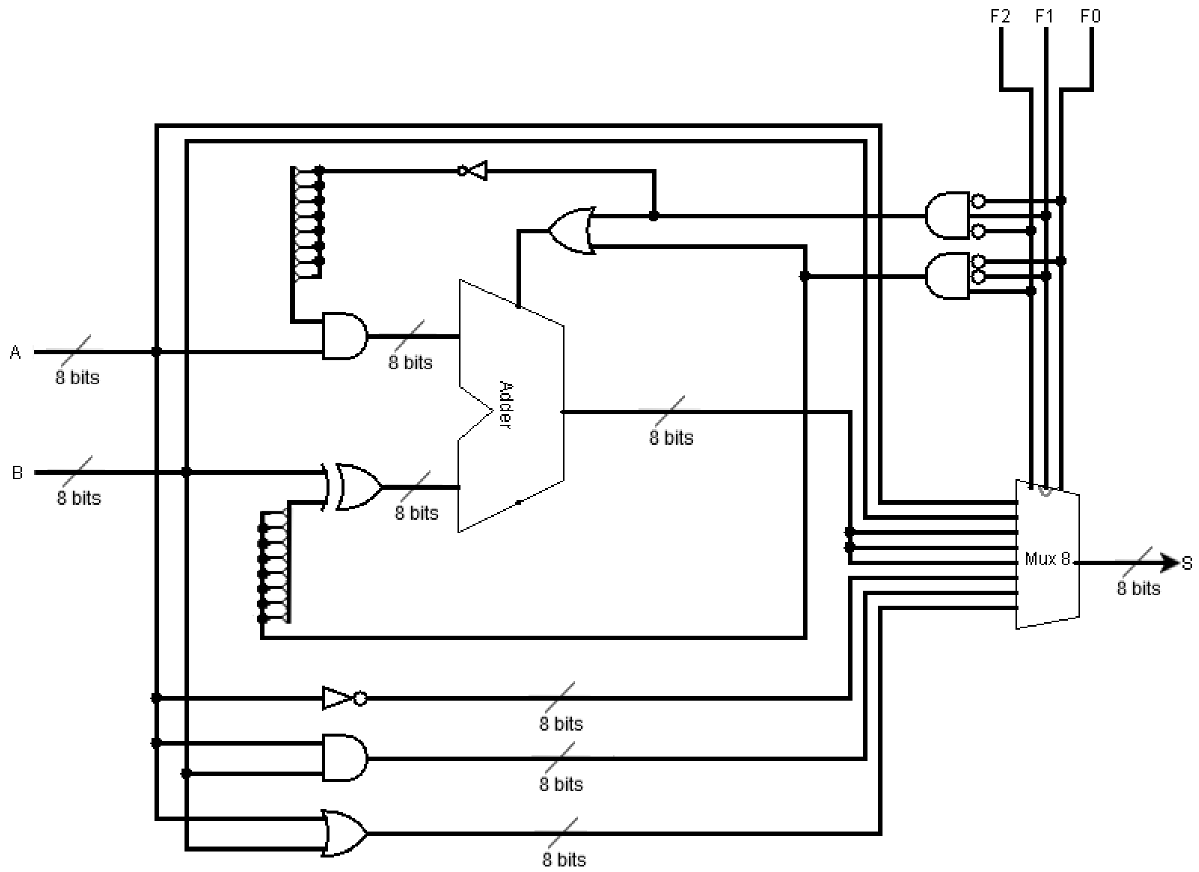


The diagram of the complete ALU is as follows :



Input 0 and input 1 of the Multiplexer take values of A and B respectively. Input 2 of the Multiplexer is that of the B+1 function, it is implemented by the addition of 0+B with the Previous Carry put to 1, which is the same as B+1. Input 3 is the A+B addition with Previous Carry put at 0. Input 4 for the subtraction of A-B is implemented by the addition of A+(-B), since we are in 2's-Complement (-B) is B (bit-wise which is the 1's-Complement) +1 achieved by the Previous Carry set to 1. Inputs 5, 6 and 7 of the Multiplexer are respectively NOT, AND and OR bitwise.

2) The optimization will be done on the operations B+1, A+B and A-B, each one using an Adder. Knowing that a single Adder has a high number of gates (8 x 5 = 40 gates). We will optimization the ALU by using only one Adder instead of 3 for the 3 operations.



The 2 AND gates following the Functions entry (F2,F1, and F0), make it possible to detect respectively the operation B+1 and A-B, if in the Functions entry they detecet the code of B+1 (010) or of A-B (100) the corresponding gate will emit a 1. The OR gate at the input of the Previous Carry of the Adder will use the output of the 2 ANDs and supply the Adder with +1 if the operation is B+1 or A-B, and 0 if it is A+B (following the same reasoning of the previous non-optimized UAL).

The AND gate in the 1st entry of the Adder allows to choose bit by bit to enter the value 0 during the B+1 operation or the value of A for A+B and A-B. This choice is controlled by the 1st AND which detects B+1. As a reminder the choice is made by the AND gate such that if it receives a 0 in one of its entry it emits a 0 as an output, and if it receives a 1 it emits the value of the 2nd input (A in our case).

For the 2nd entry of the Adder, the XOR is uesd to preform the 1's-Complement if necessary. If the XOR receives a 0 from the AND detector of A-B it don't change the value of B, but if it receives 1 it performs the 1's-Complement bit by bit on B, which becomes $\overline{B}$. This behavior comes from the logic of the XOR gate (To be checked on the XOR truth table), if one input of a XOR is at 0 the output would be the same as the 2nd input, and conversely if one input is at 1, the output would be the 1's-Complement on the 2nd input.

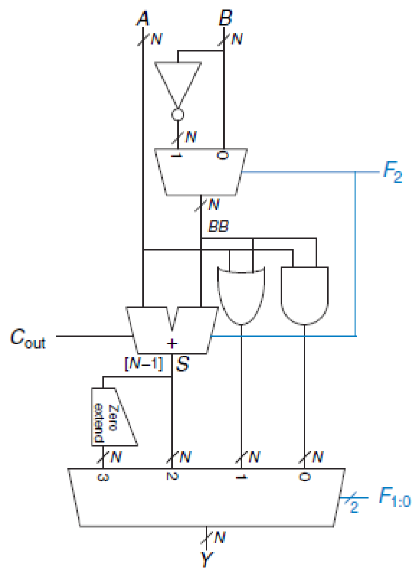
3) We can observe that the Multiplexer at the bottom only has 4 inputs controlled by 2 bits F1 and F0. F2 allows to control another Multiplexer on input B, if F2=0 it is B that is used on the rest of the ALU, otherwise it is B (1's-Complement) which is used. Thus the table of functions is subdivided into 2 parts, for F2=0 the 1st half of the operations use B, including A AND B, A OR B and A + B implemented respectively bitwise by an AND, OR gate and a Adder. While for F2=1 the 2nd half uses $\overline{B}$, including A AND $\overline{B}$, A OR $\overline{B}$ and A – B, which are also implemented on the AND gate, OR and the Adder.

It is the F1 and F0 that make the Multiplexer at the bottom to choose the operation to take on a given half of the table. Then for the A-B operation, and considering the 2's Complement encoding, it is implemented as A+($\overline{B}$+1), the +1 is provided as Previous Carry (called C_{in} in the book) of the Adder, by F2 which is set to 1 for this operation. We can note that the C_{out} (or Next Carry) represents an additional output for the ALU.

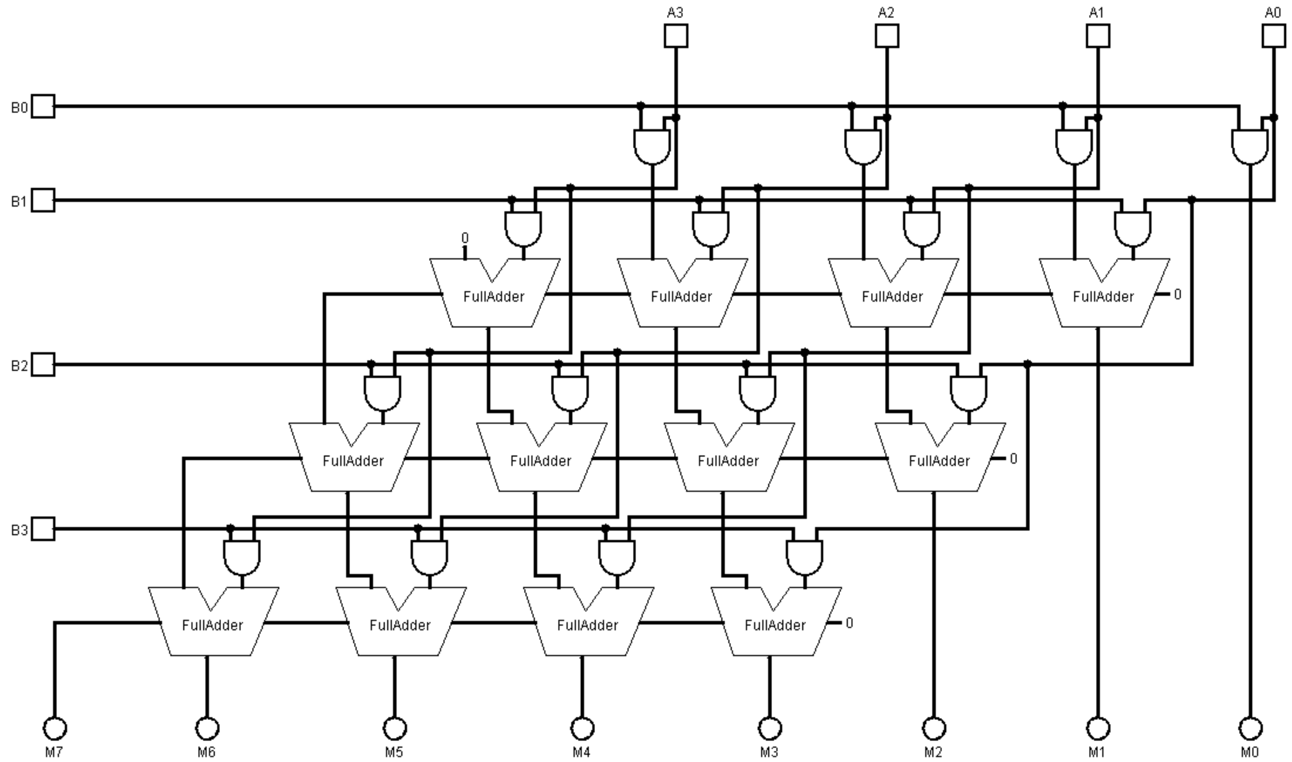
The SLT (Set-to-1 if Less Than) operation performs the Less-than comparison operation using subtraction. So to know if A<B, the UAL performs A-B, and takes the last bit [N-1] which represents the *sign* bit. Then the ALU extends the bit over N bits with the Zero-Extender by adding 0s, in this way if A-B is negative the output in the last position of the Multiplexer would be 00...01 on N bits, and if the result is positive the output would be 00..00. Of course the same operation for F2=0 has no meaning, this is why it was *not-used* in the table. Actually N in the book is up to 32 bits.

Table 5.1 **ALU operations**

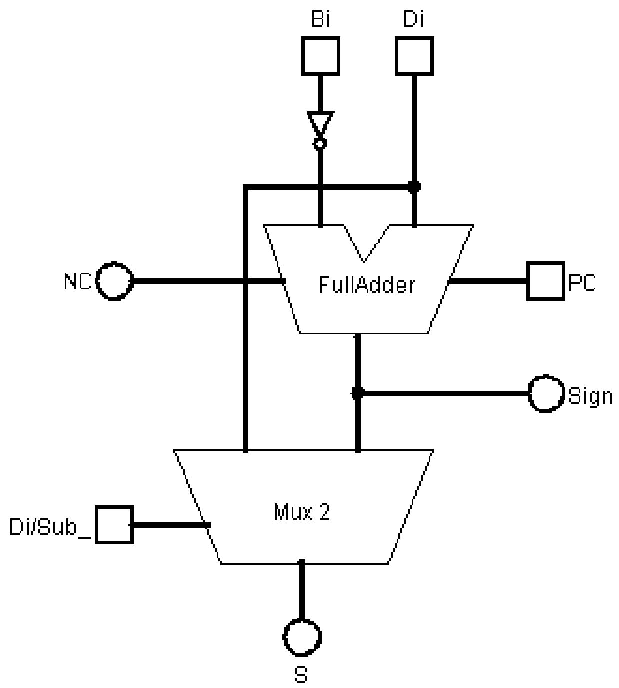
$F_{2:0}$	Function
000	A AND B
001	A OR B
010	A + B
011	not used
100	A AND $\overline{B}$
101	A OR $\overline{B}$
110	A – B
111	SLT



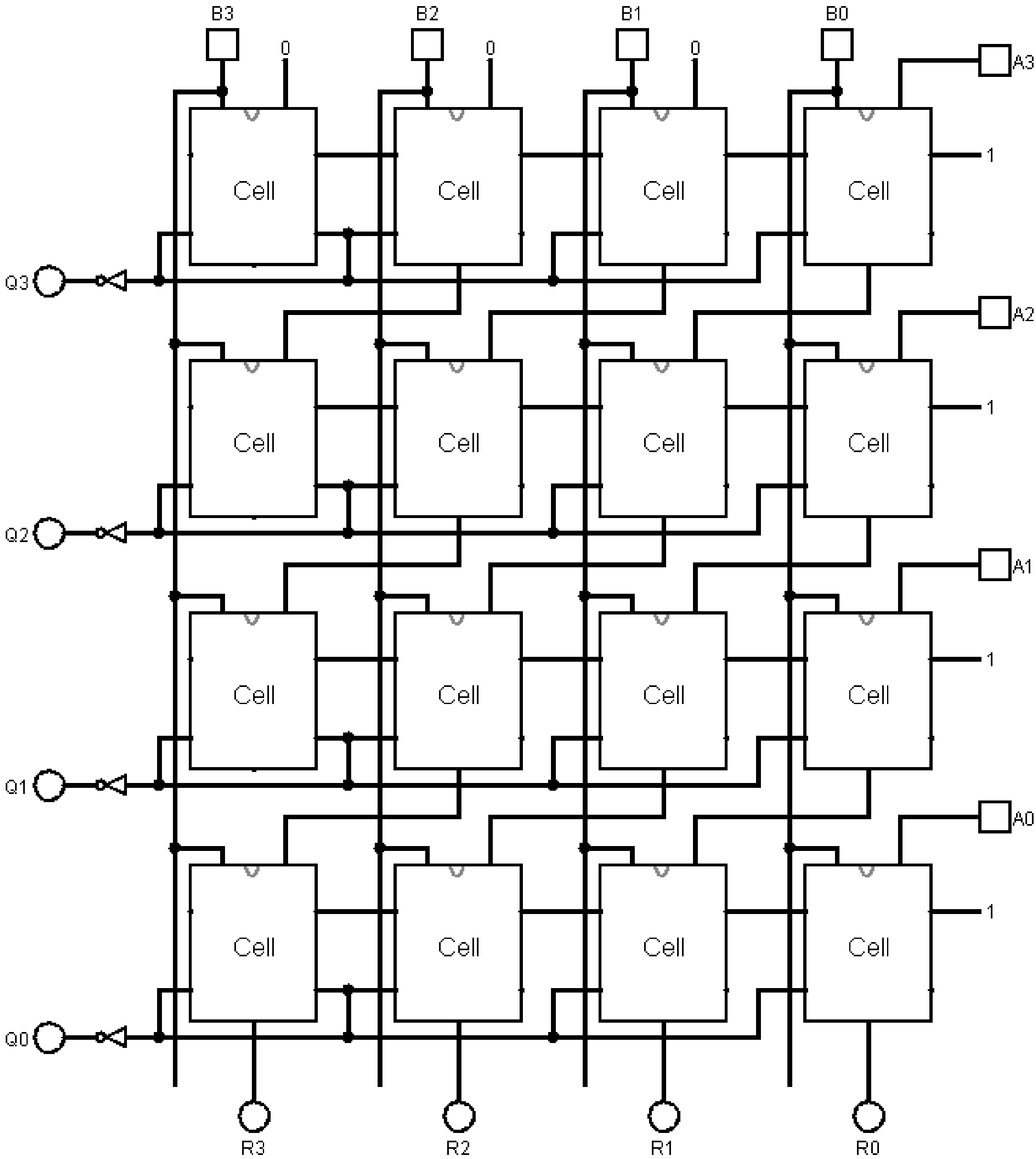
4) The Multiplier :



The Divider :



One Cell



Remark : Sub_ in the Cell entry name is actually $\overline{\text{Sub}}$. In the hardware design literature we can also find formats equivalent to the bar such as Sous_{bar} or Sous_{b}.